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MS-7681

ATX(Full Size)
Ver: 0A

CPU:

INTEL - Sandy Bridge LGA 1155

System Chipset:

INTEL - Cougar Point PCH

OnBoard Chipset:

Clock Gen:IDT 4106
HD Audio Codec:RTL892
LAN:RTL 8111E 10/100/1000 NIC X 2
SIO:FIN71889AD
ESATA Controller: JM363
USB3.0: UPD720200F1
Flash ROM: 64 Mb SPI (PCH)
1394 Controller: VT6308P

Main Memory:

DDRIII (1066/1333MHz) * 4 (Dual Channel)

Expansion Slots:

PCI Express (X16) Slot * 2
PCI Express (X1) Slot * 3
PCI Slot * 2(From IDT TSI383)

PWM:

CPU:UPI6234(5PHASE)
CPU_VTT:UP6113A(1PHASE)
CPU_SA:UP6113A (1PHASE)
DDR/PCH PWR:UP6103A

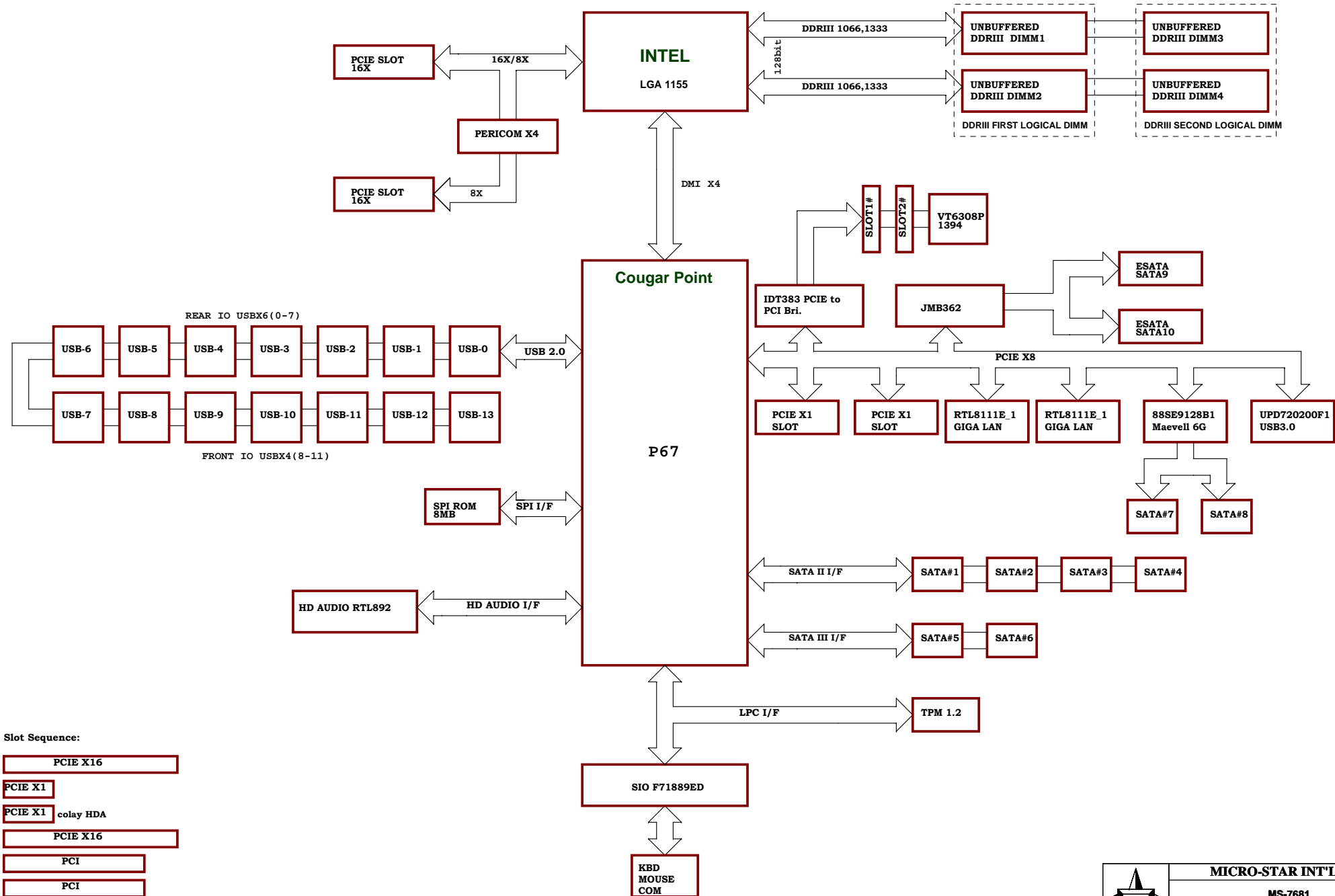
Other:

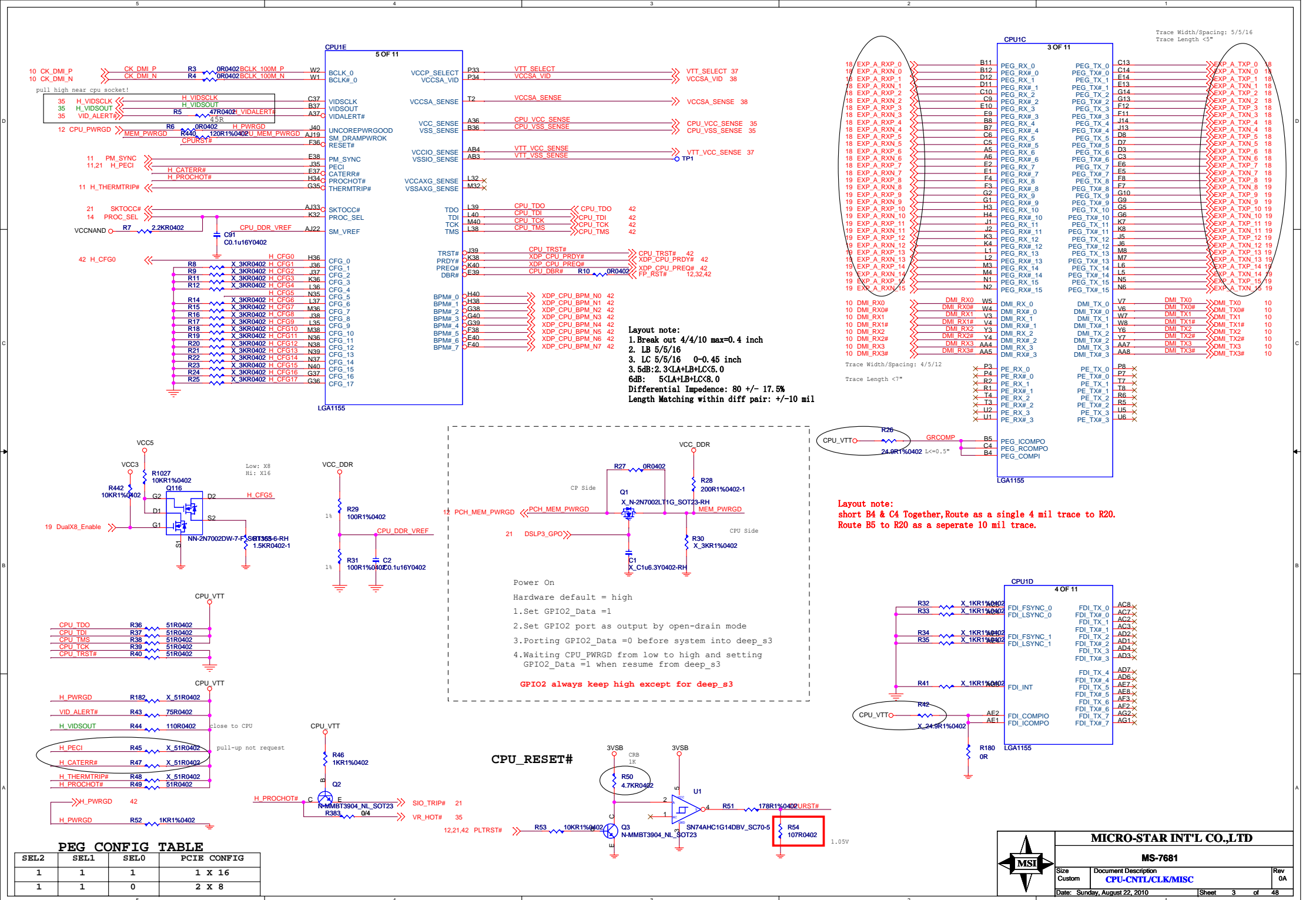
SATA3.0 x2+SATA2.0 x4 (PCH)
ESATA2.0 x2 (JMB363)
USB2.0 *4 (Rear*8 Front*4)
COM Header *1
USB3.0 *4 (Rear*2 Front*2)

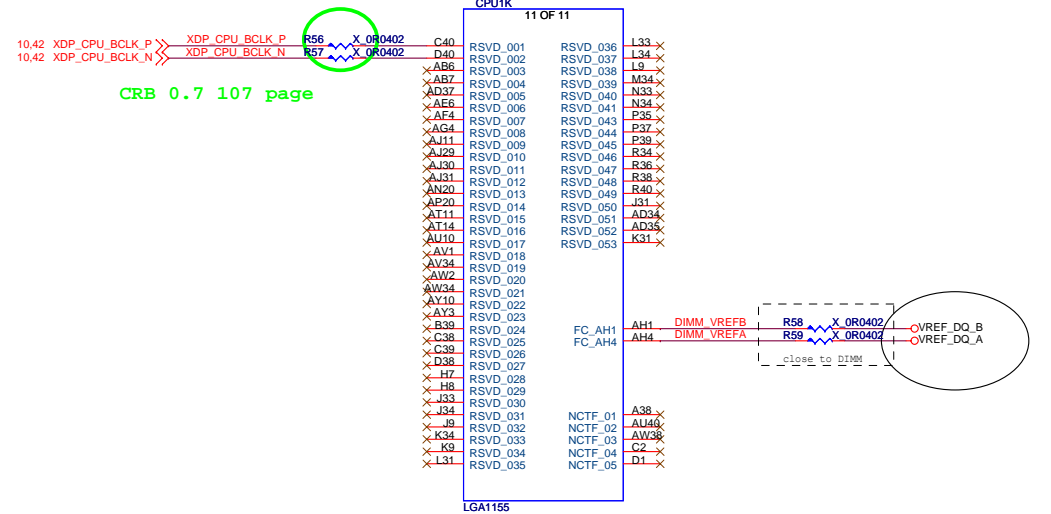
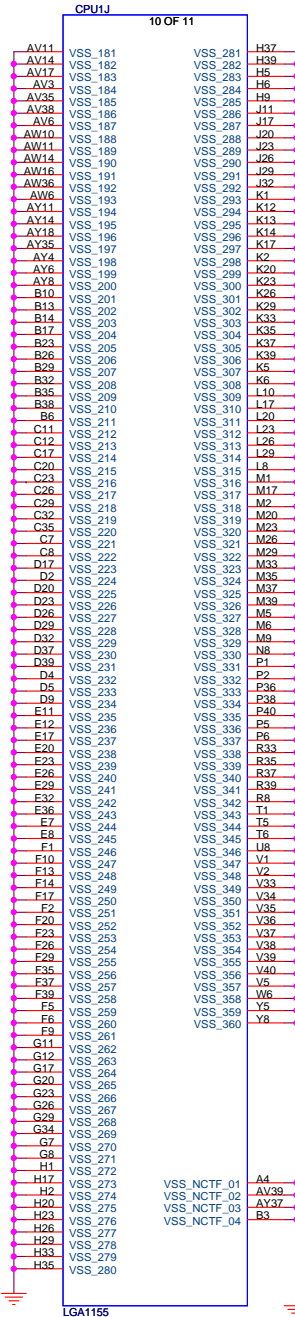
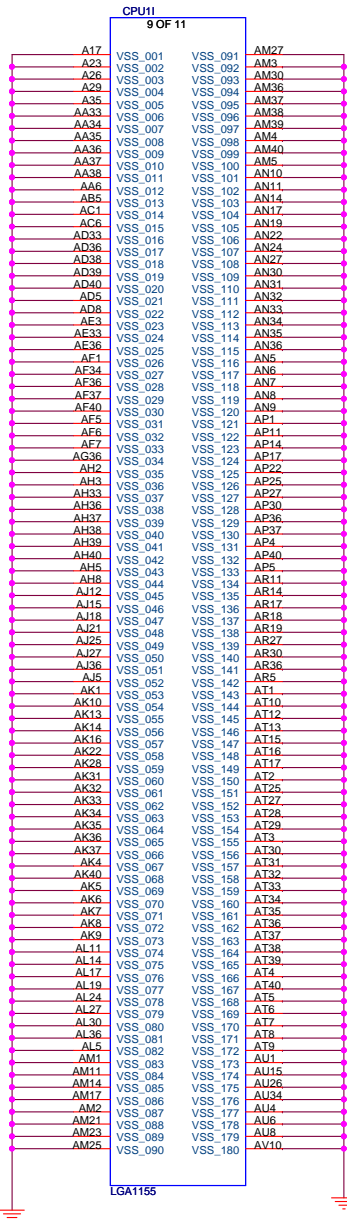
ACPI:

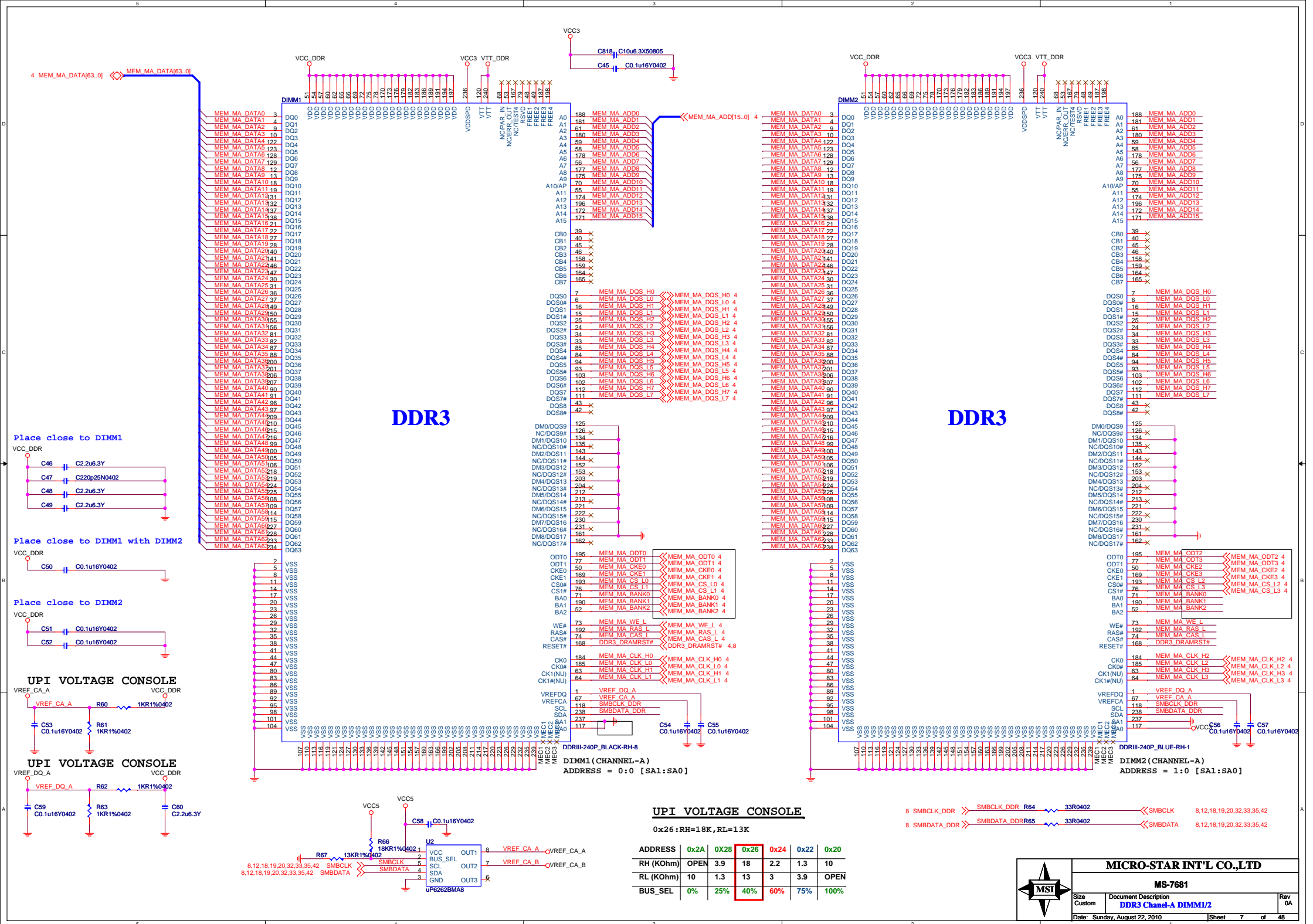
UPI





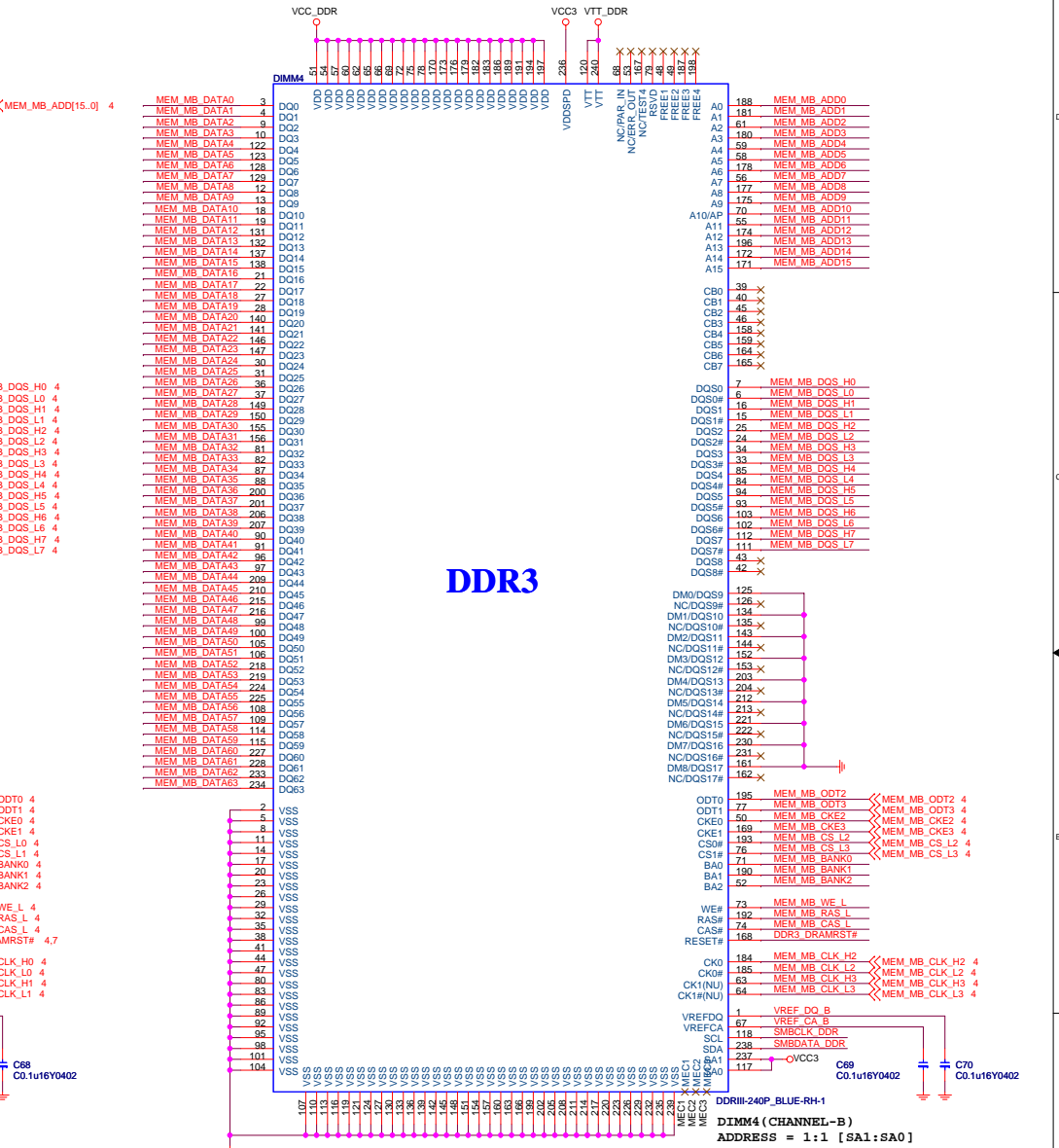
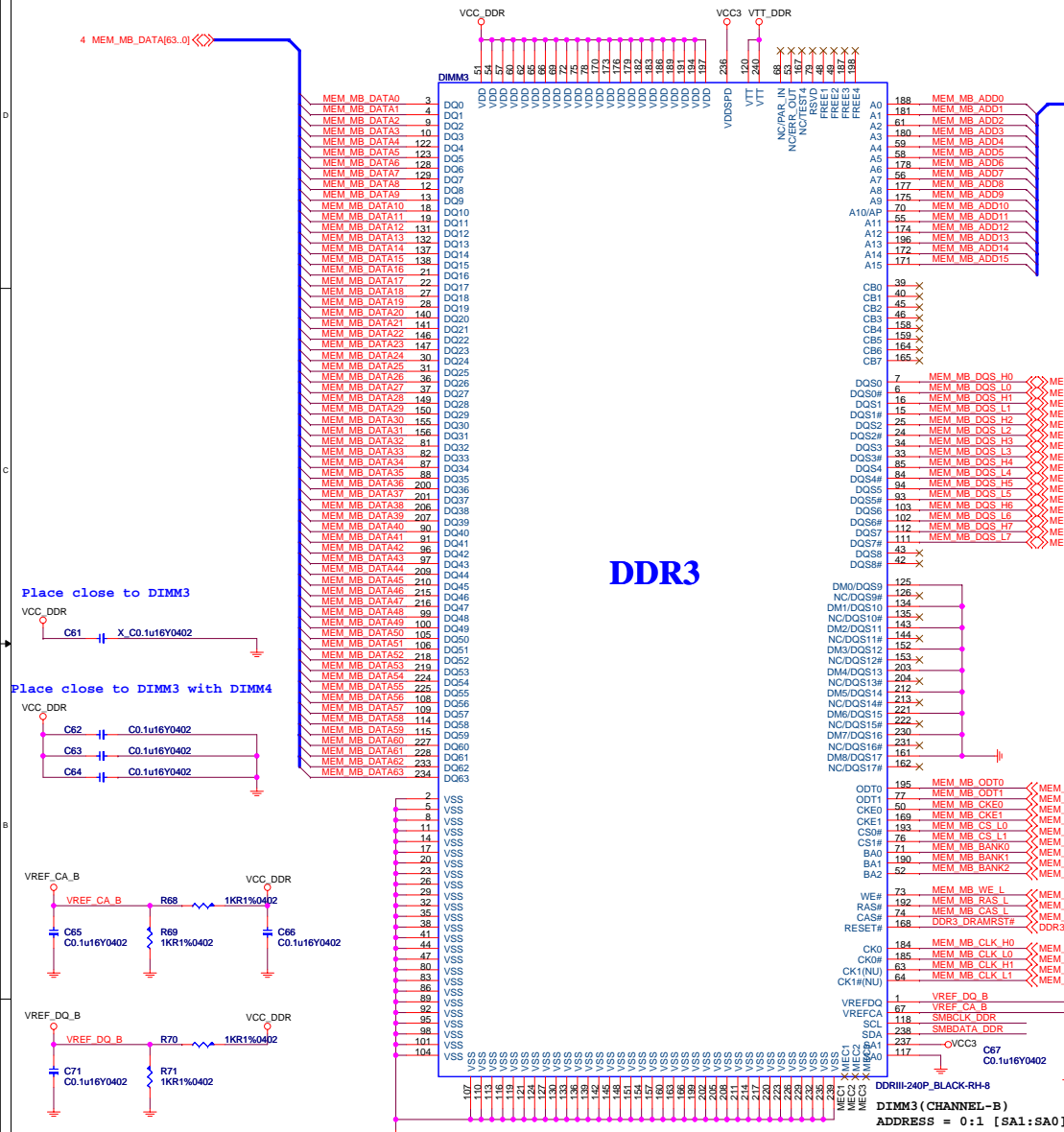






DDRIII DIMM_B0

DDRIII DIMM_B1



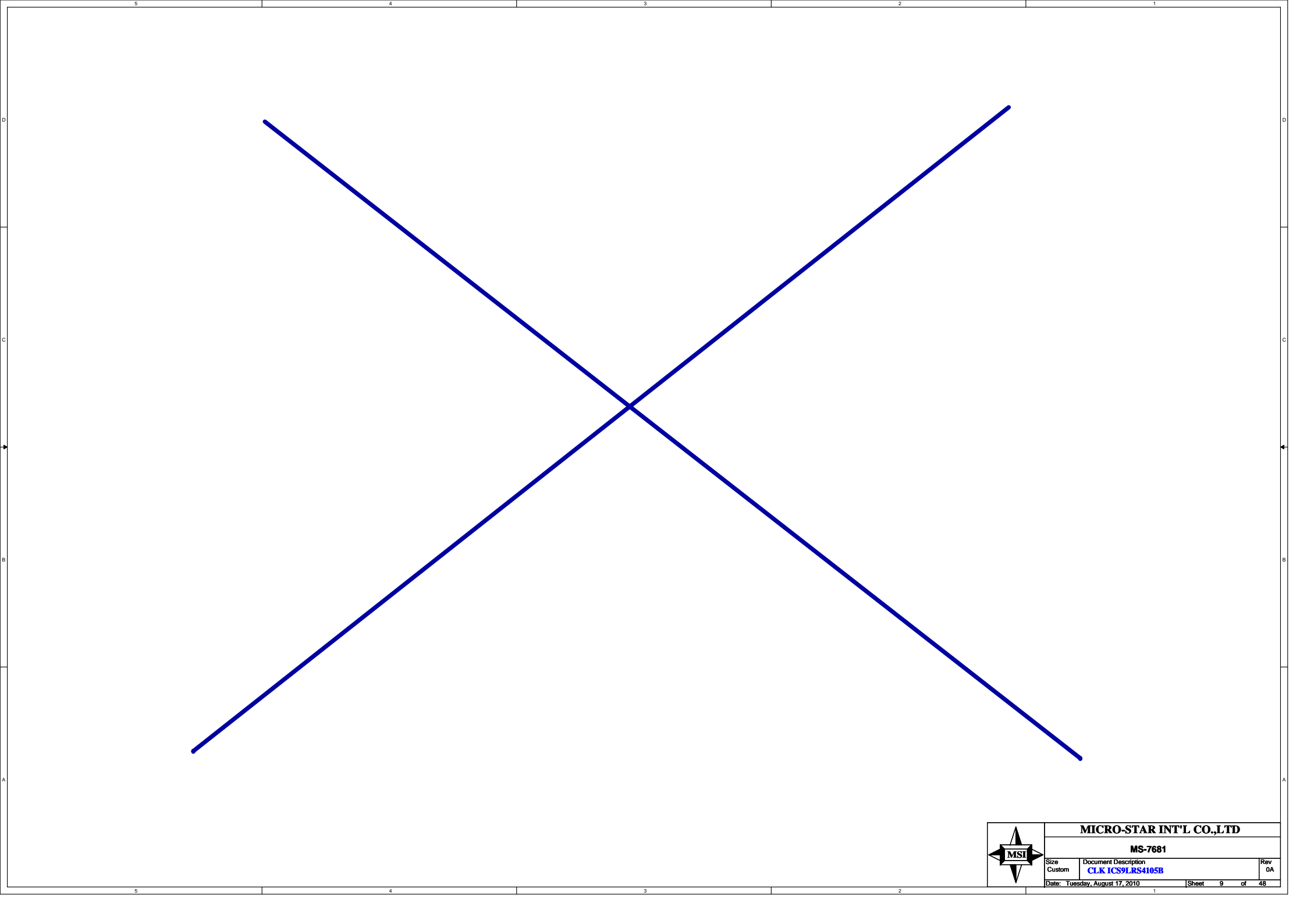
UPI VOLTAGE CONSOLE


0x28:RH=9.1K,RL=3K

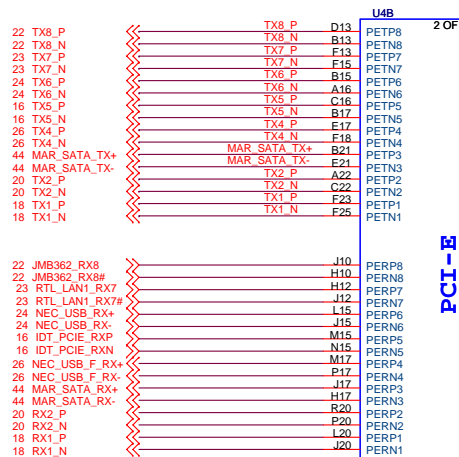
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	9.1	3	2.2	1.3	10
RL (KOhm)	10	3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



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MS-7681		
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Custom	DDR3 Chnel-B DIMM3/4	0A
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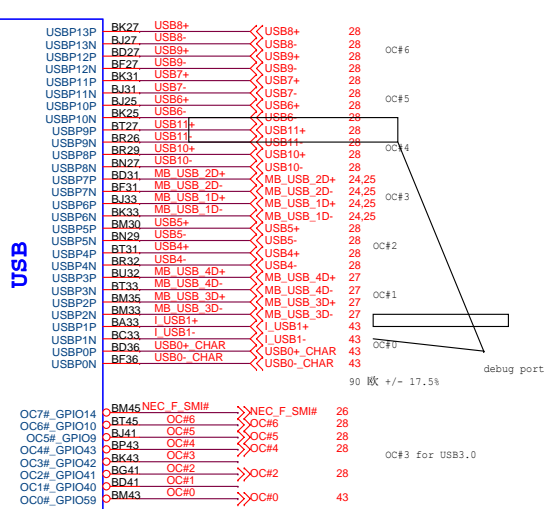


			MICRO-STAR INT'L CO.,LTD		
			MS-7681		
Size	Document Description			Rev	
Custom	CLK ICS9LR54105B			0A	
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PCI - E

DMI

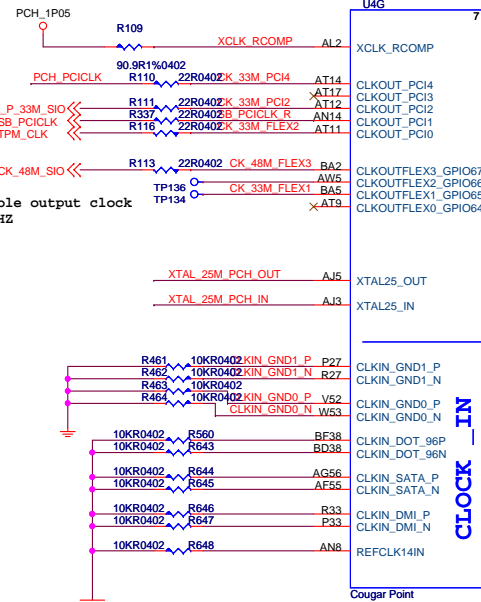


Cougar Point

PCI

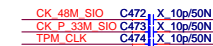
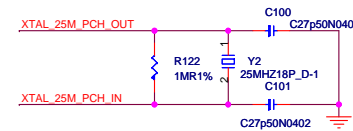
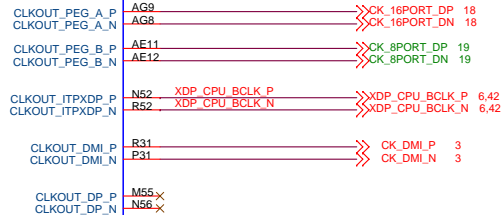
DG: 8.2K PU

Programmable output clock to 33/48MHZ



CLOCK

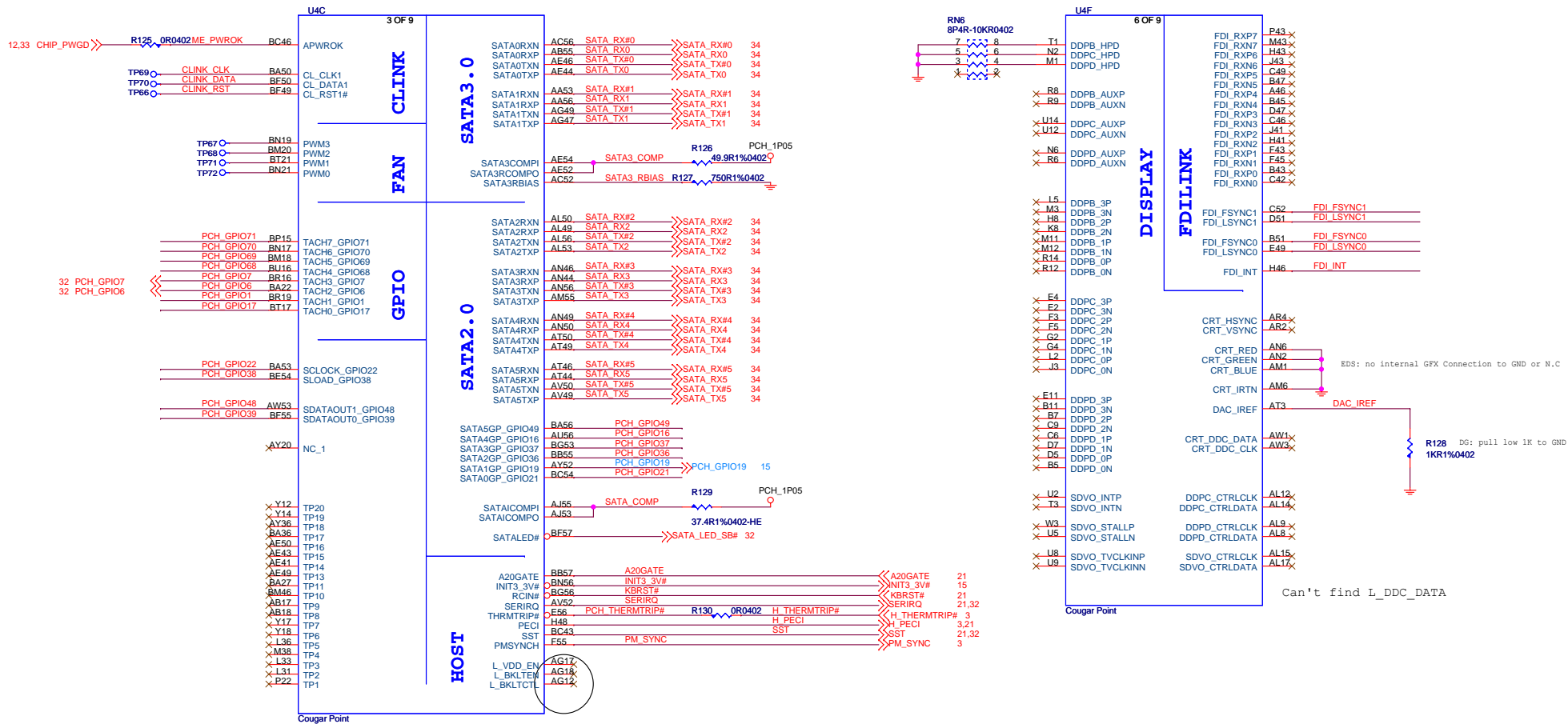
CLOCK_IN



MICRO-STAR INT'L CO.,LTD

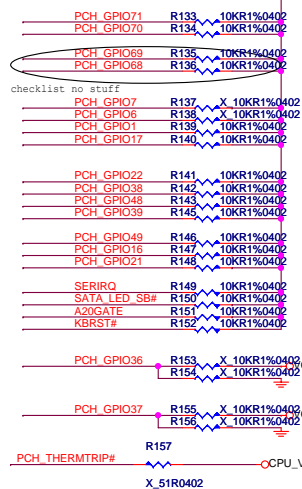
MS-7681

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Custom	IBEXPEAK-PCI-E/DMI/USB/CLK	0A
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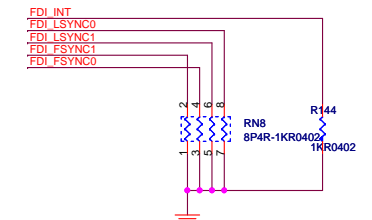


Pull HIGH for

PCH



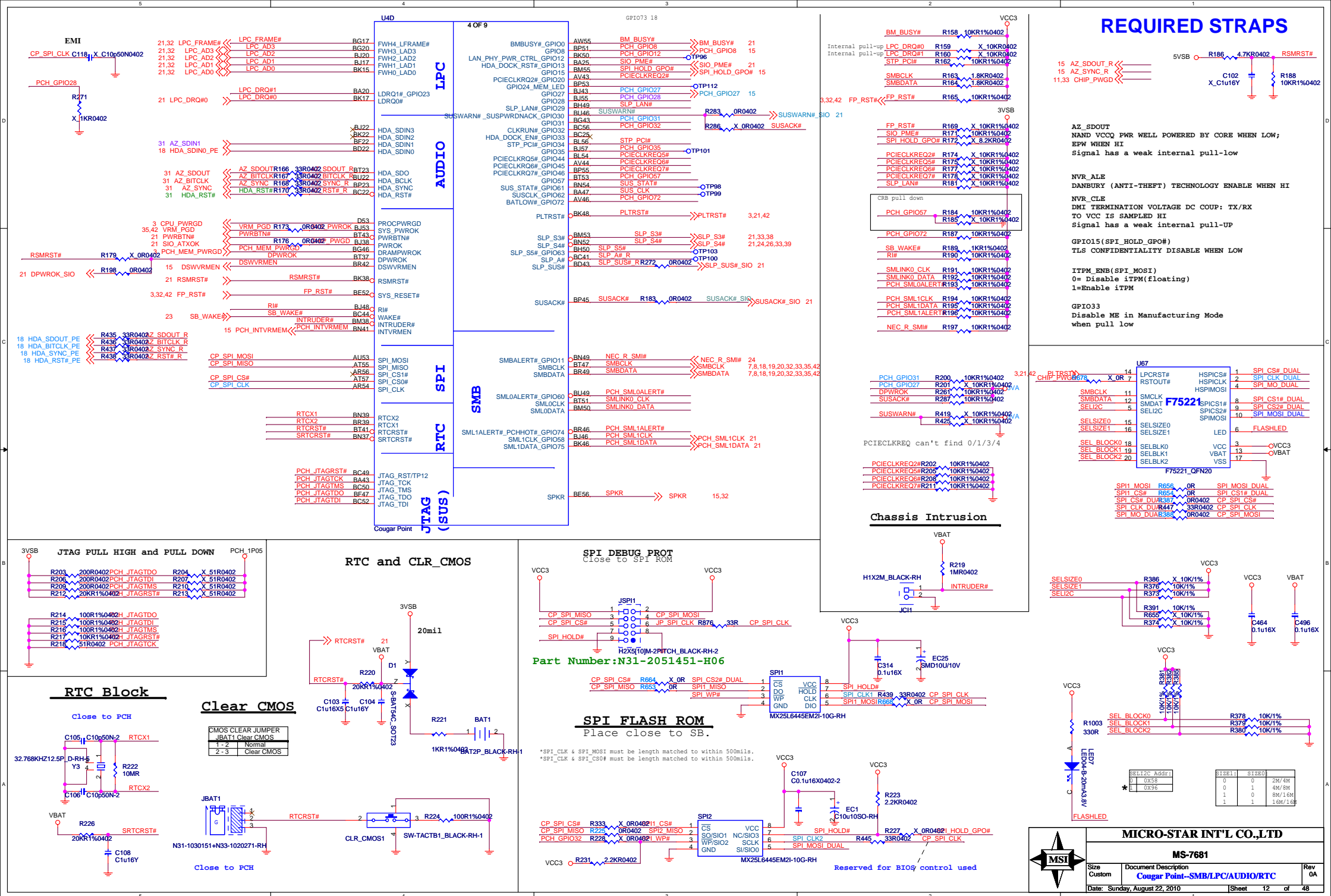
No VGA(FDI 1Kohm pull down)

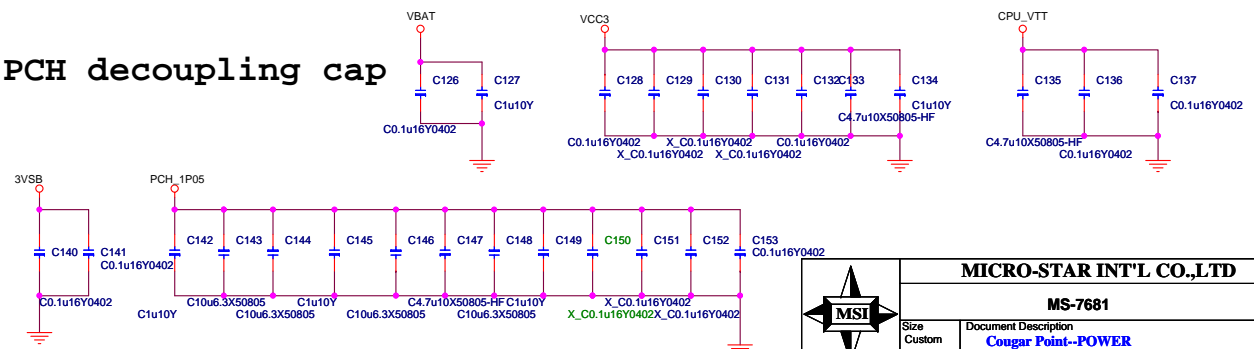
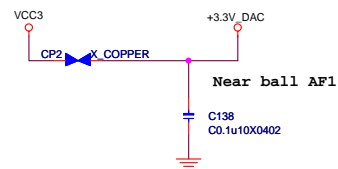
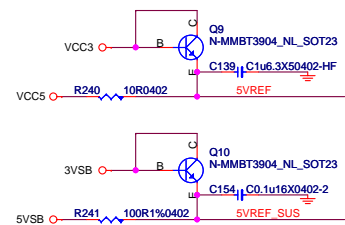
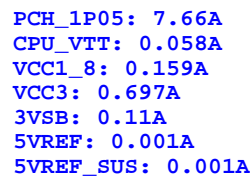


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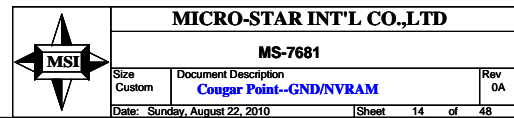




MICRO-STAR INT'L CO.,LTD

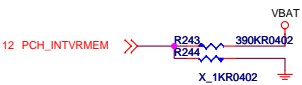
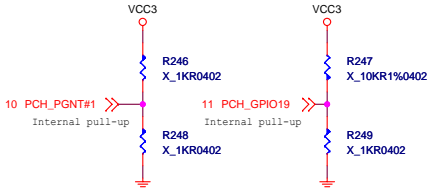
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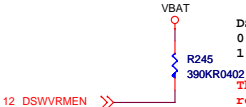
PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



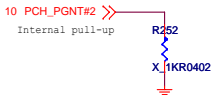
INTVRMEN
0: DISABLE INTERNAL VRM
1: ENABLE INTERNAL VRM *

When these voltage regulators are enabled, the integrated GbE only operates at 10/100 Mbps during S3-S5.

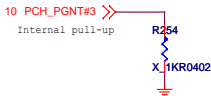


DSWVRMEN
0 : Disable Internal Deep Sleep 1.05 V regulators.
1 : Enable Internal Deep Sleep 1.05 V regulators.

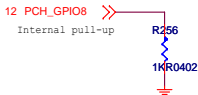
This signal enables the internal Deep Sleep 1.05 V regulators. Must beconnected even when not supporting DSW.



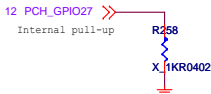
DMI AC/DC MODE
0 : AC
1 : DC *



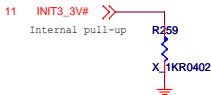
Topblock swap override when pull-low
Signal has a weak internal pull-up



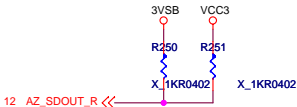
GPIO8
0 : Integrated Clocking Enable (FCIM)*
1 : Buffer Through Mode Enable (BTM)



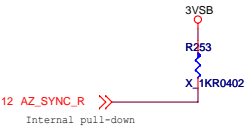
GPIO27
0 : OD PLL VR disabled
1 : OD PLL VR enabled *
Signal has a weak internal pull-up



INT3_3V#
0 : INIT3_3V to asserted for 16 PCI clock to reset theprocessor by some evens occur
1 : Can not to reset the processor



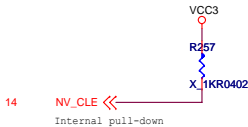
HDA_SDO
Disable ME in Manufacturing Mode
when pull LOW ????



HDA_SYNC
OD PLL VR SUPPLY SEL
0: 1.8V SUPPLY *
1: 1.5V SUPPLY



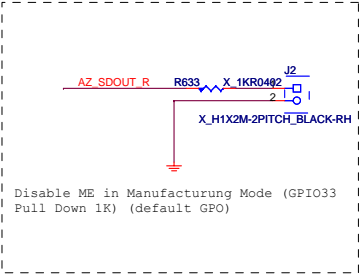
GPIO15
0 : TLS CIPHER SUITE WITH NO CONFIDENTIALITY *
1 : TLS CIPHER SUITE WITH CONFIDENTIALITY



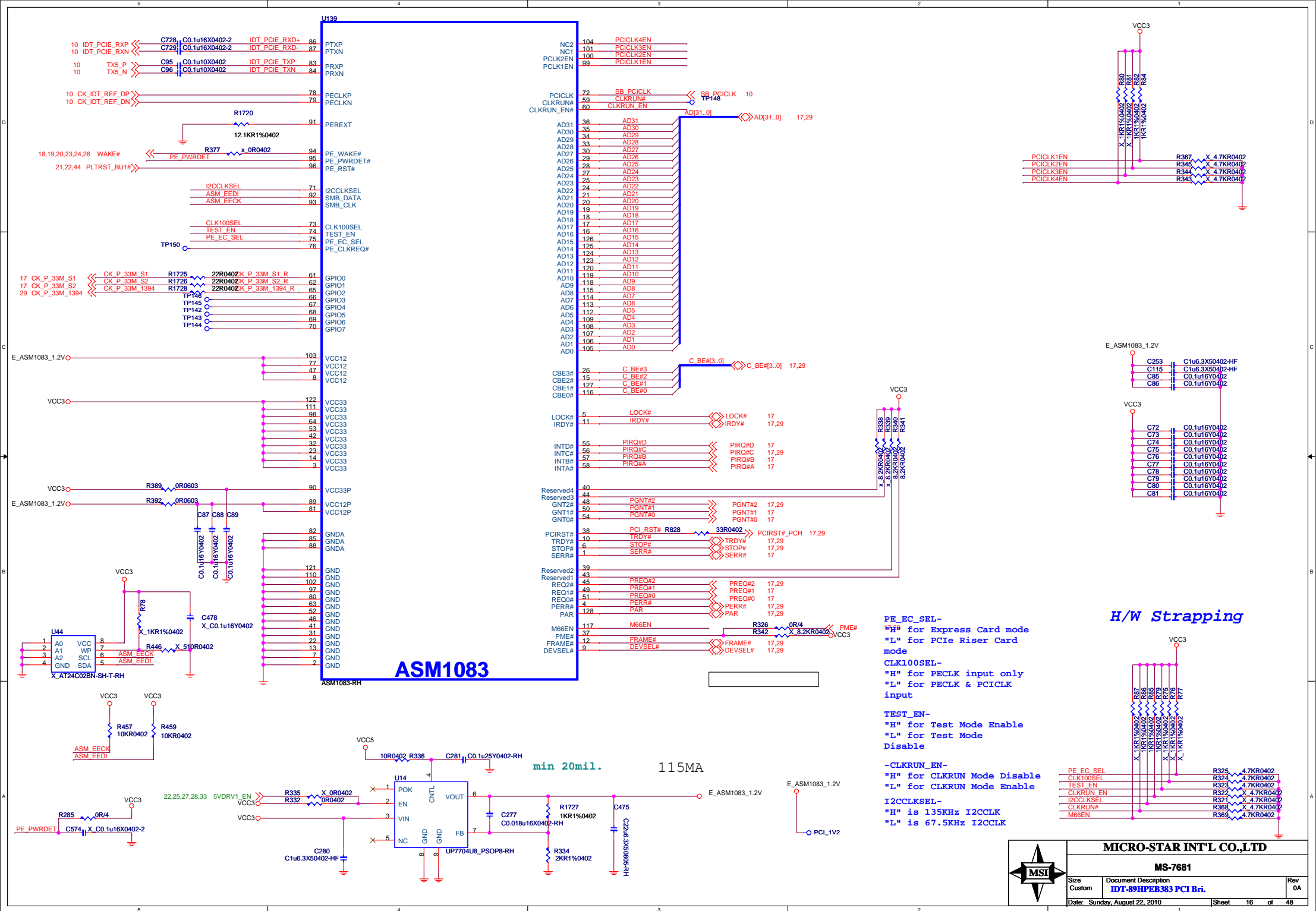
DMI/FDI TERMINATION VOLTAGE
DC COUPLED: TX/RX TO VCC ISF SAMPLED HIGH
DC COUPLED: TX/RX TO VSS IF SAMPLED LOW *?
AC COUPLED: TX SET TO VCC/2, RX SET TO VSS REGARDLESS OF THIS STRAP



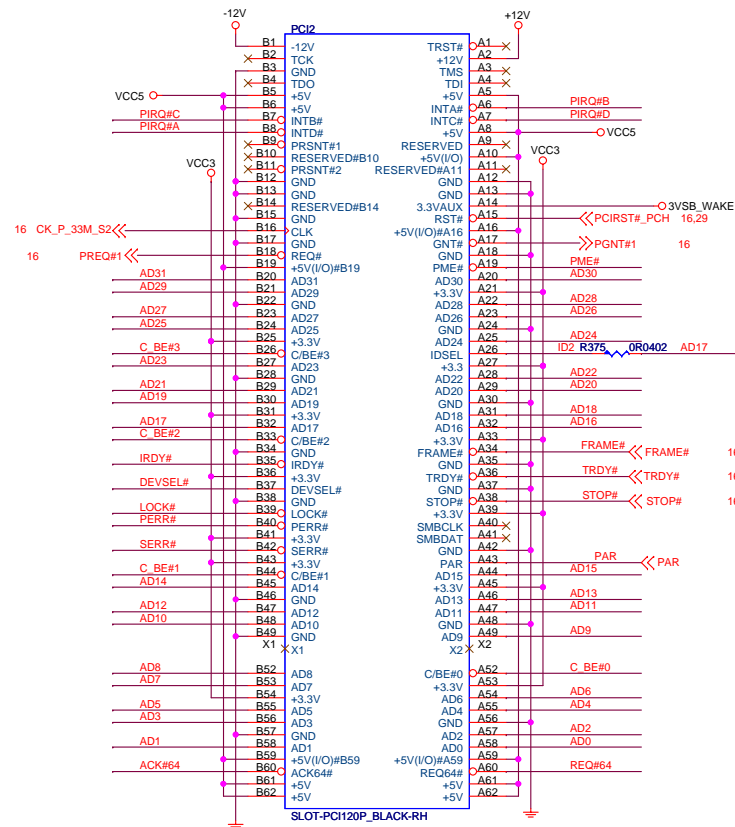
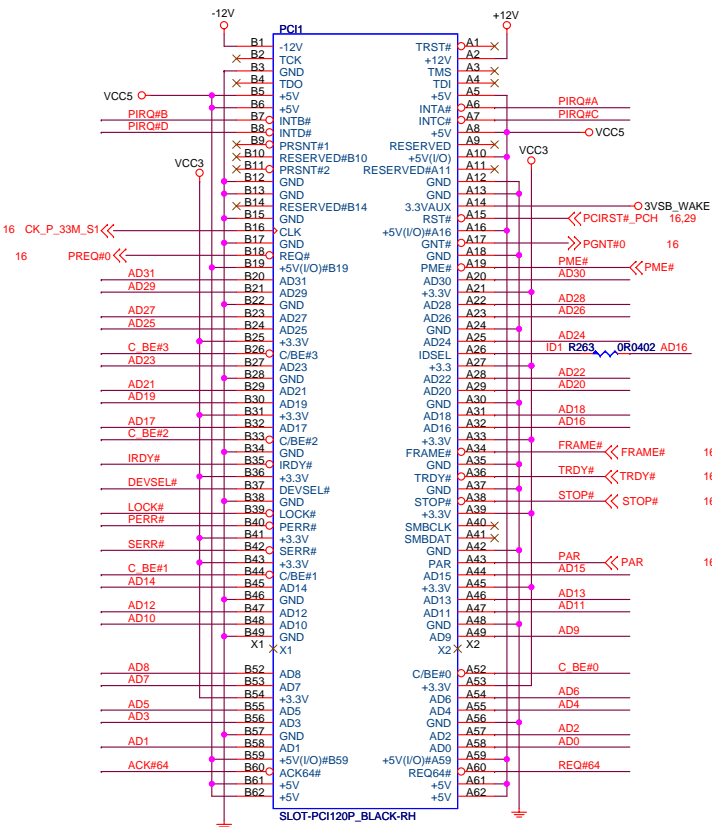
SPKR
0 : EN TCO REBOOT *
1 : DIS TCO REBOOT



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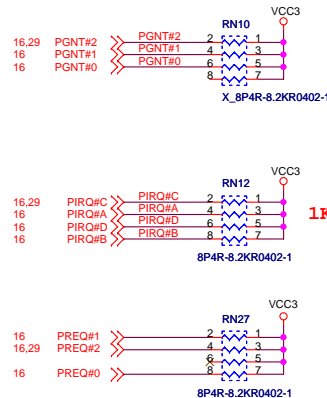
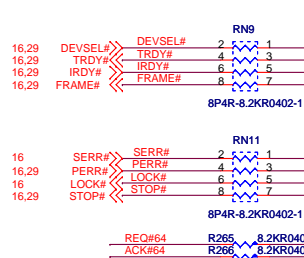
PCI SLOT 1 (PCI VER: 2.2 COMPLY)



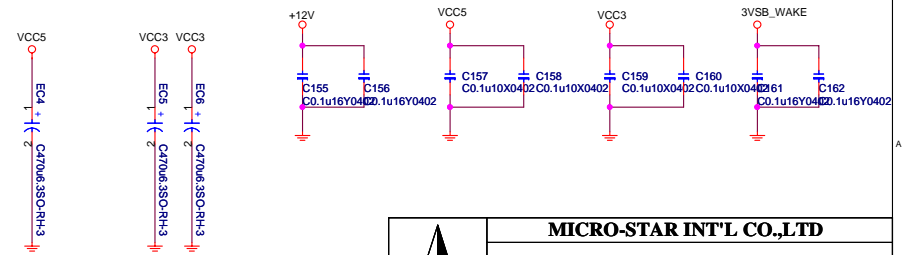
IDSEL = AD16
MASTER = PREQ#0
PIRQ#A

IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

PCI PULL-UP / DOWN RESISTORS



PCI SLOT DECOUPLING CAPACITORS

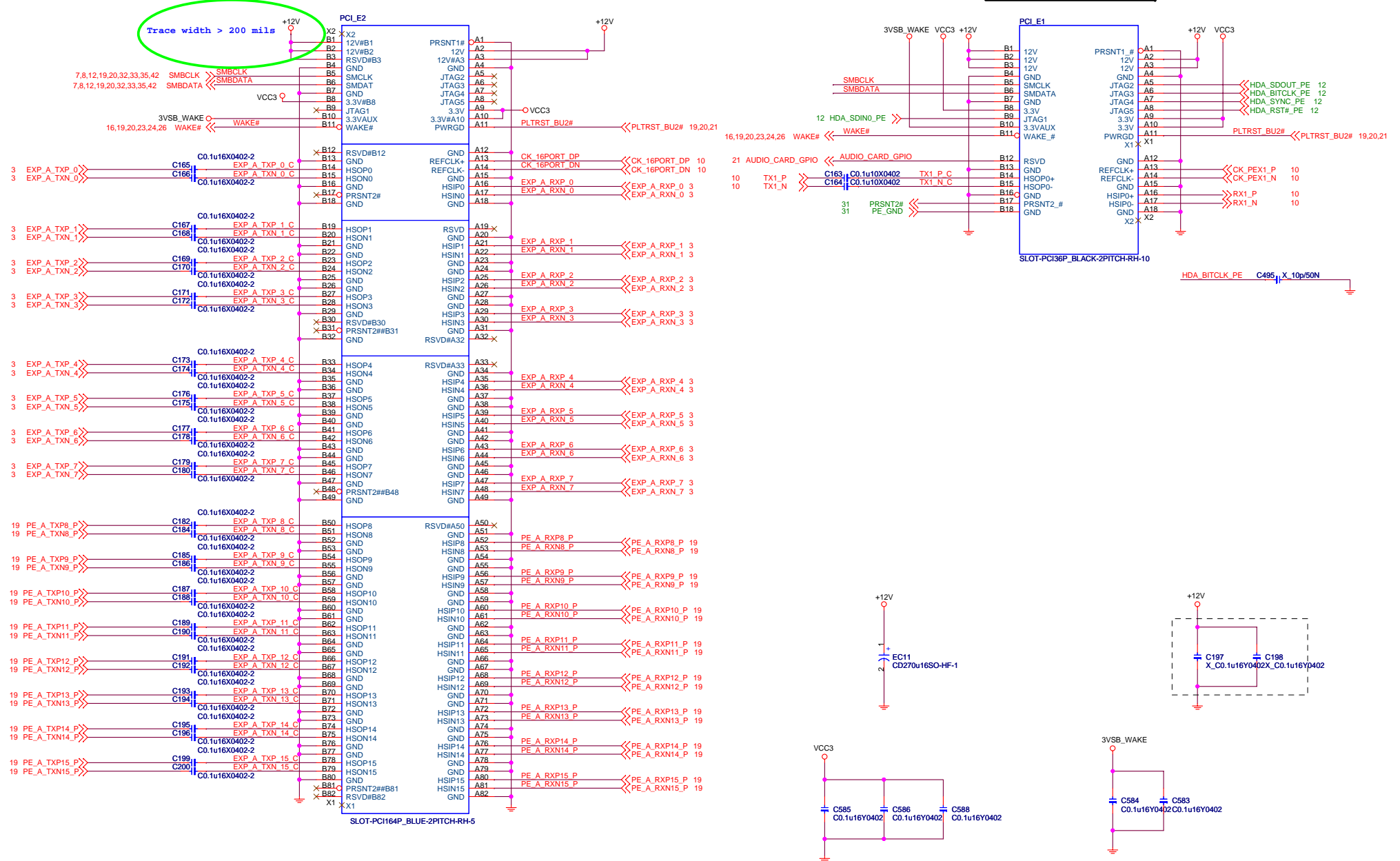


			MICRO-STAR INT'L CO.,LTD	
			MS-7681	
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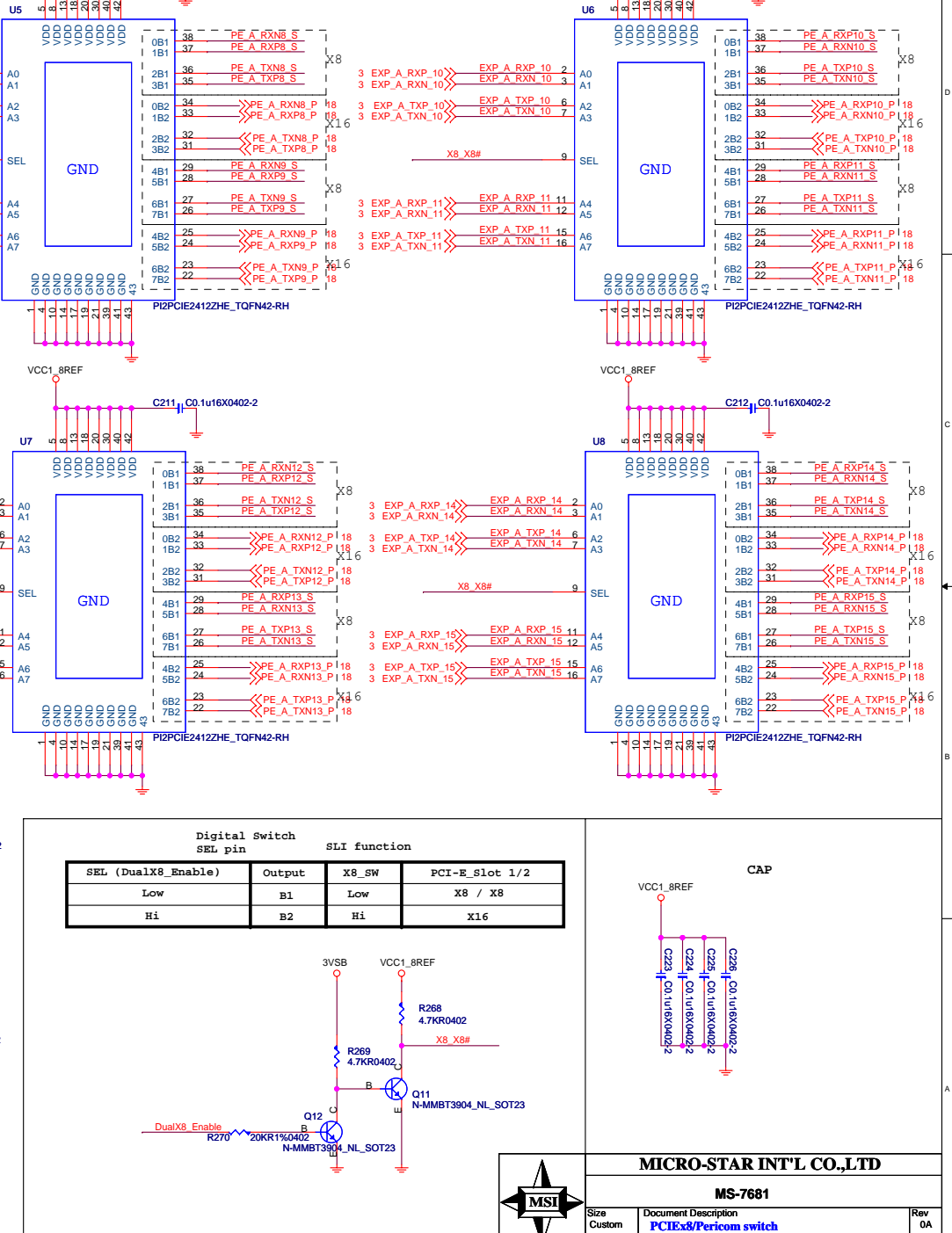
PCI_Express X16 Slot

HDA co-lay PCIe x1

PCI EXPRESS x1-PORT



Trace width > 200 mils



VCC1_8REF

C228 0.1uF 6X0402-2

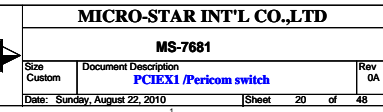
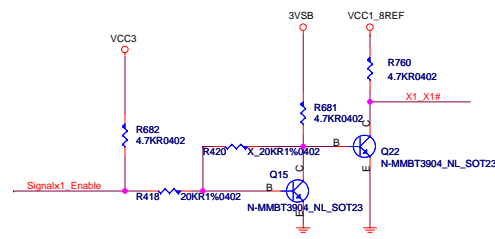
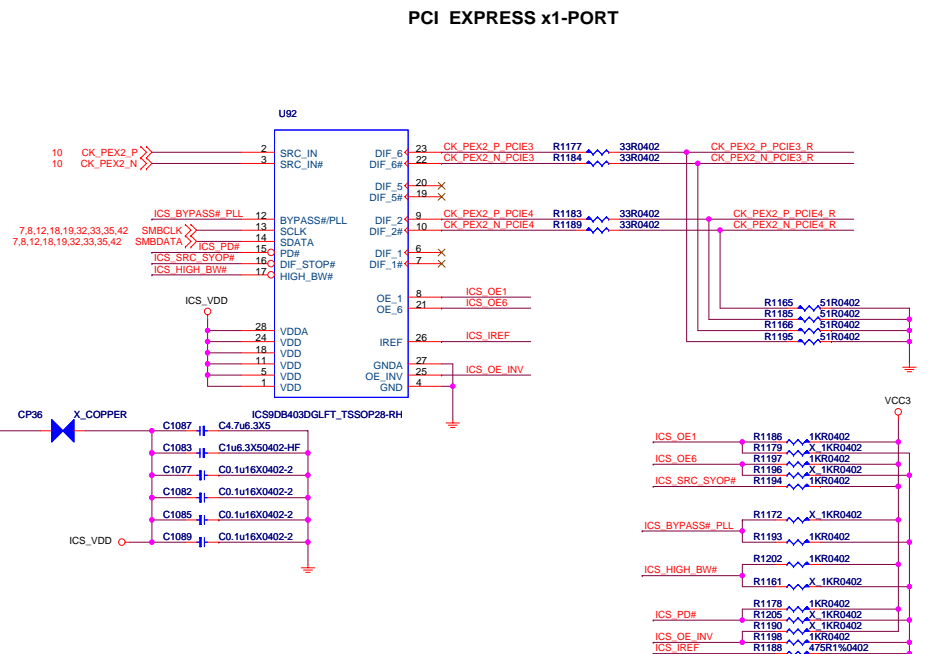
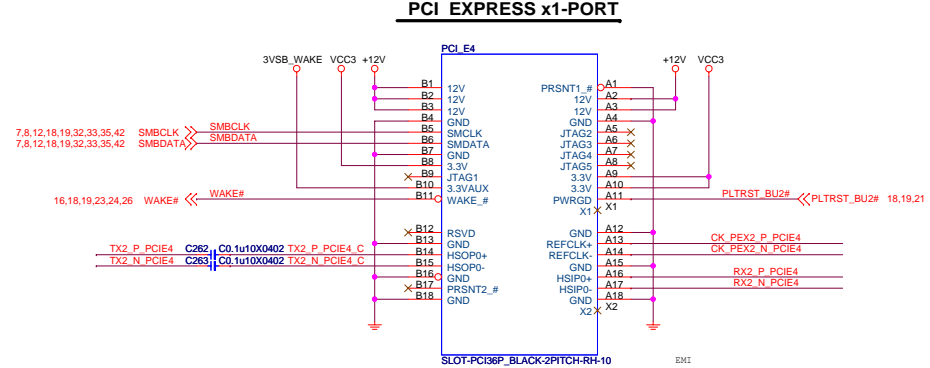
C229 0.1uF 6X0402-2

C224 0.1uF 6X0402-2

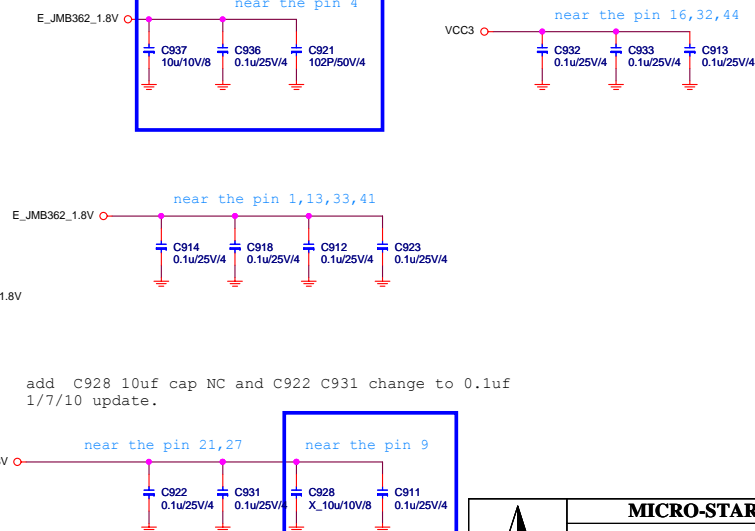
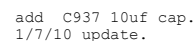
C223 0.1uF 6X0402-2

CAP





Pin4 and Pin9 over 20mil
1/7/10 update.

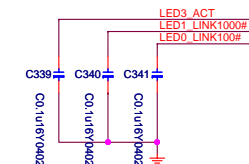
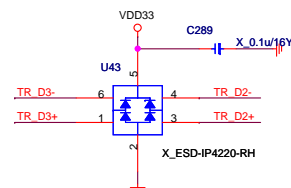
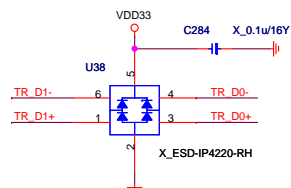
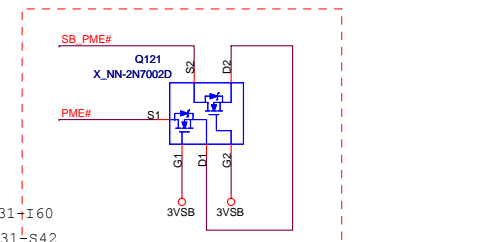
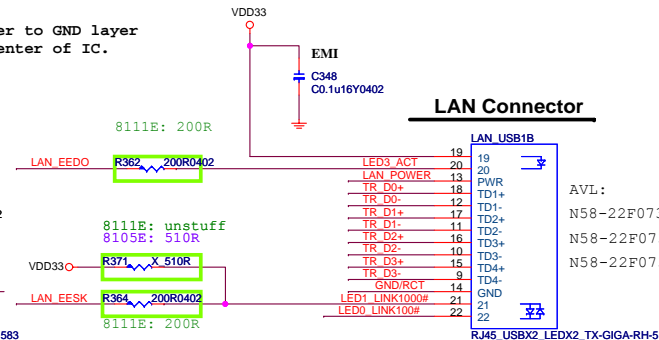
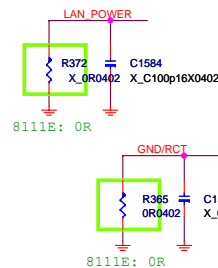
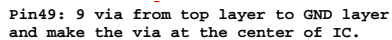
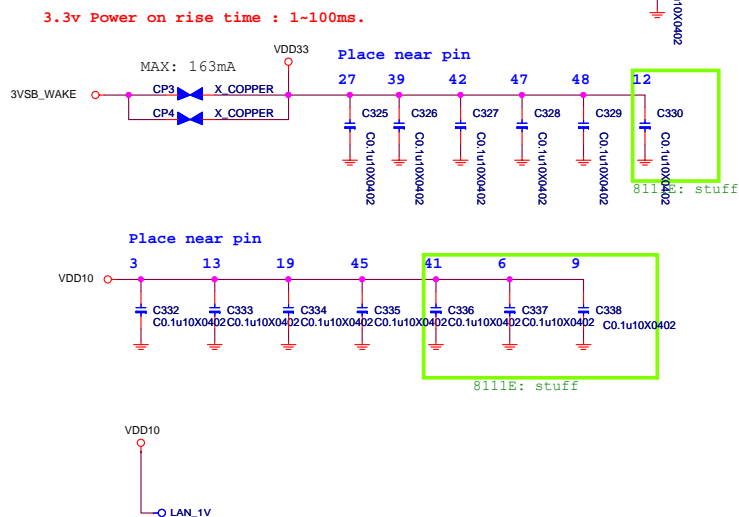
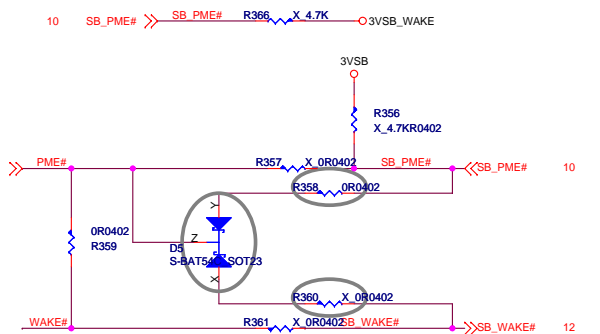
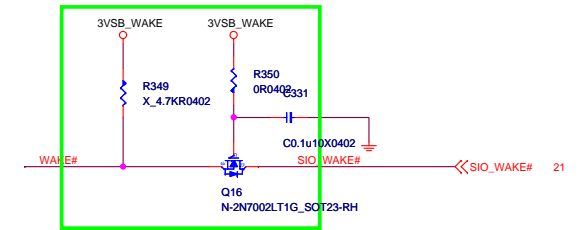
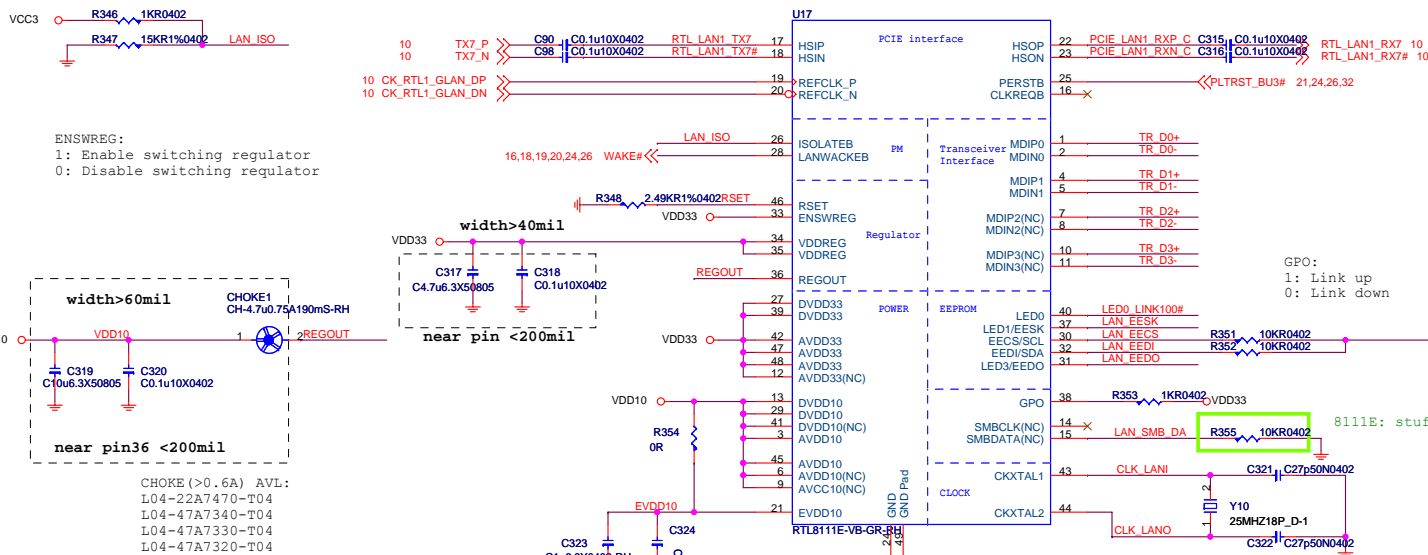


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RTL8111E Giga LAN

LAN/PCIE/PCI Wake Up CTRL Circuit



8111E POWER Consumption		
	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

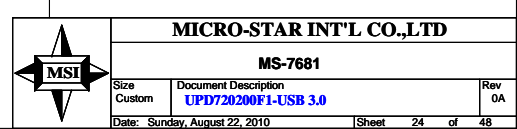
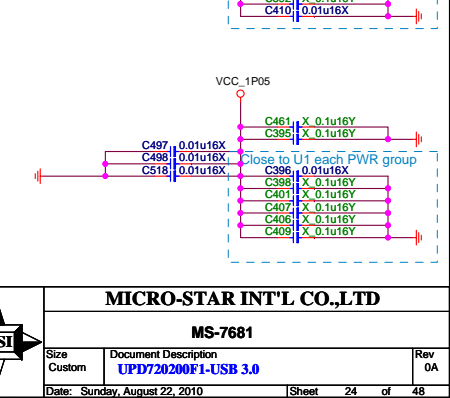
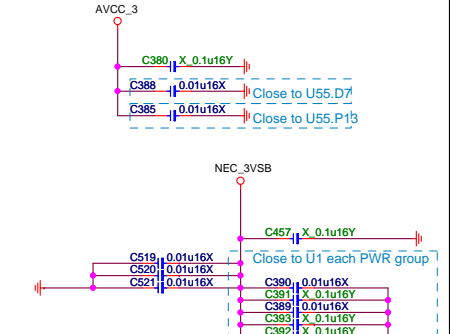
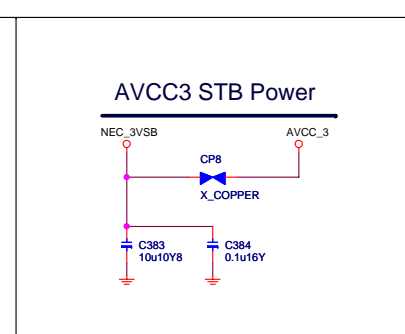
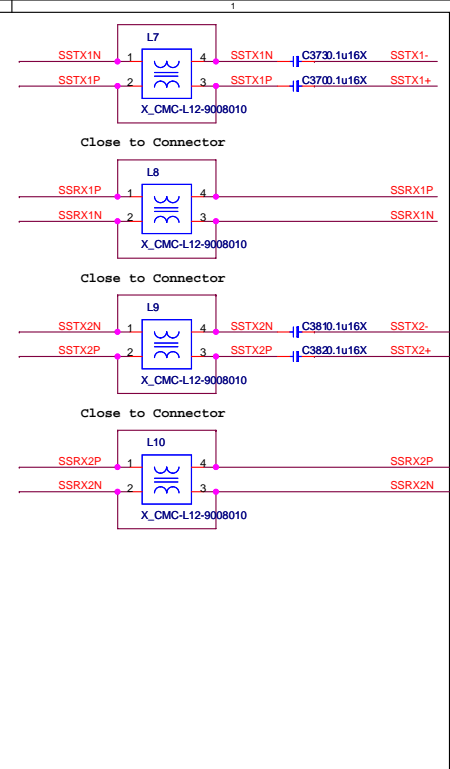
Giga-Lan		10/100-Lan	
N58-22F0731 Link Yellow Active Blinking 1000 Orange 100 Green 10 None		N58-22F0771 Link Yellow Active Blinking 100 Green 10 None	
19		19	
20	 Yellow	20	 Yellow
Orange			
21		21	
22	 Green	22	 Green

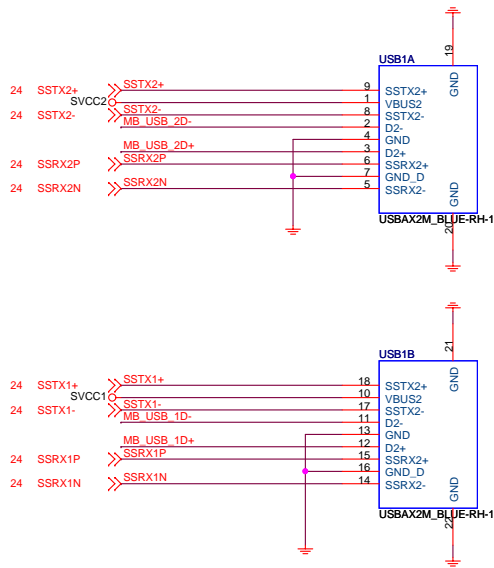


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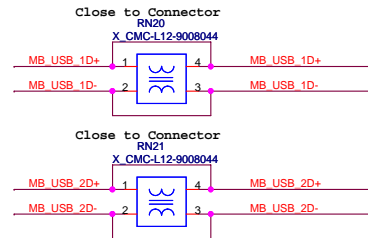
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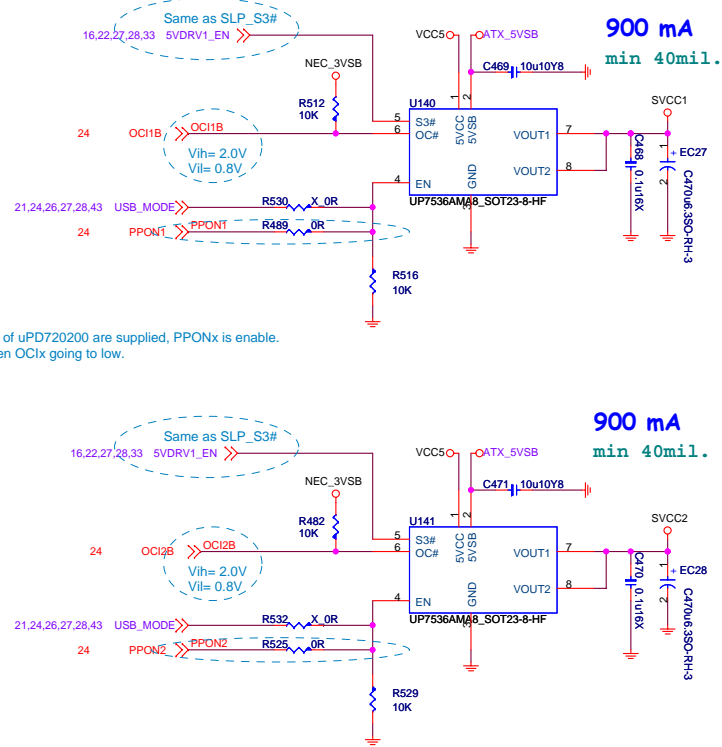




10,24 MB_USB_1D+ >>>
 10,24 MB_USB_1D- >>>
 10,24 MB_USB_2D+ >>>
 10,24 MB_USB_2D- >>>



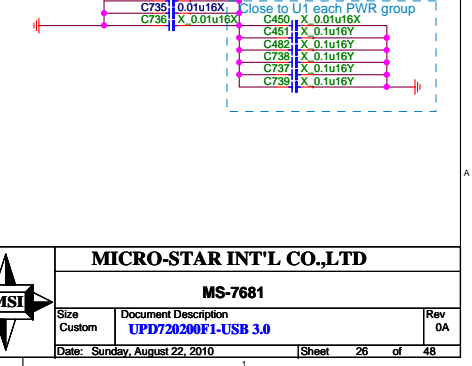
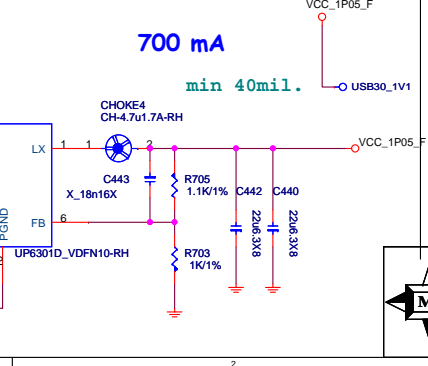
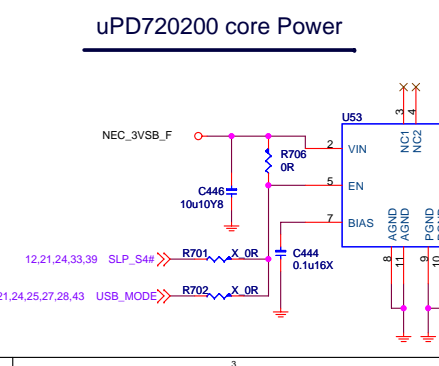
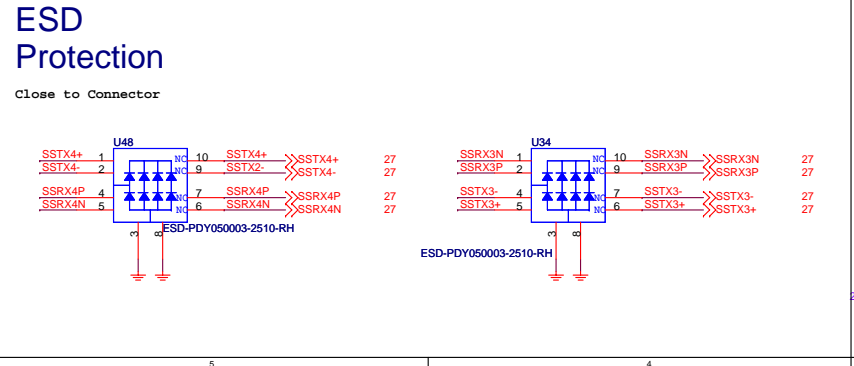
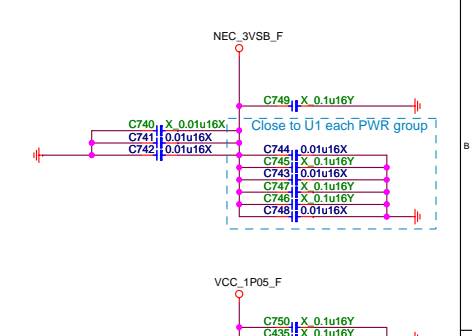
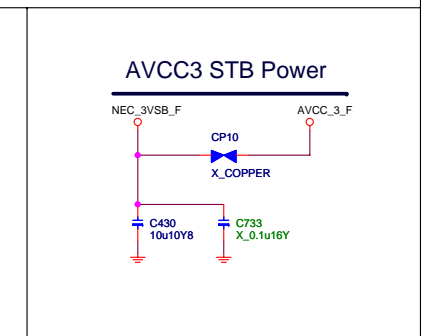
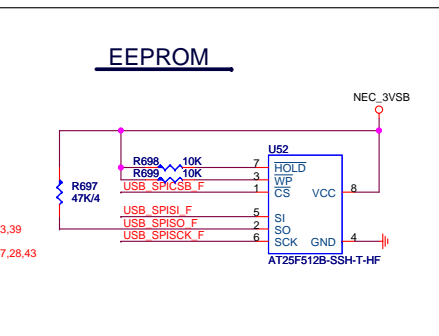
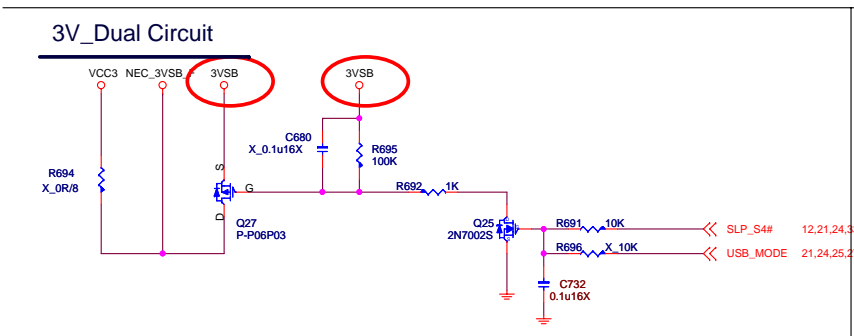
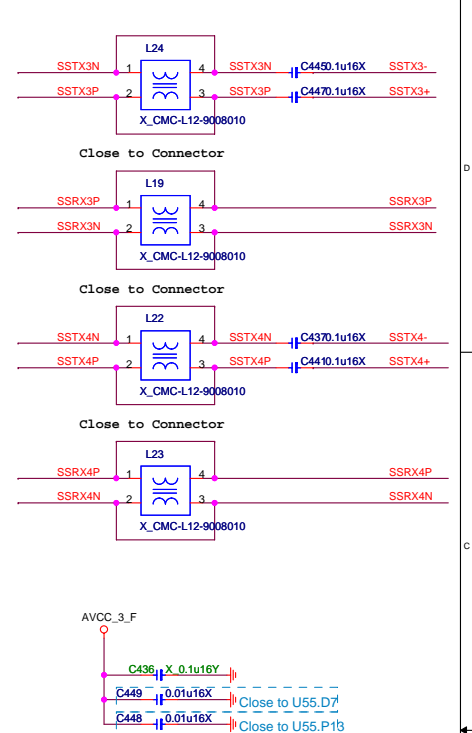
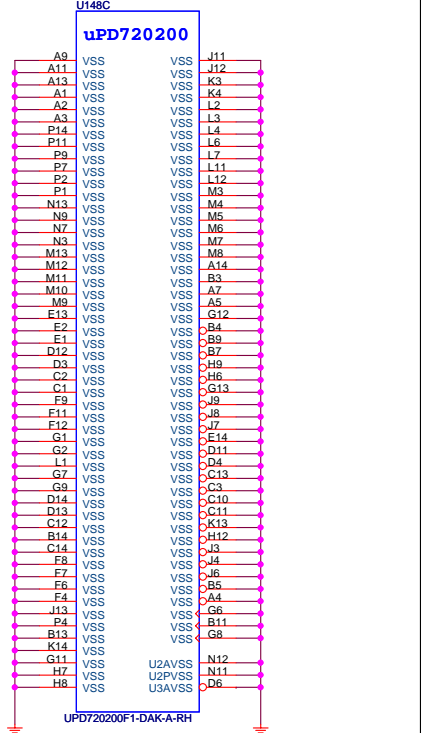
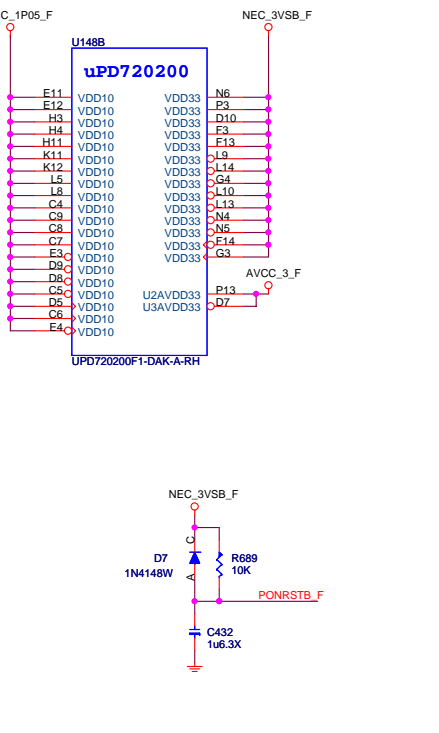
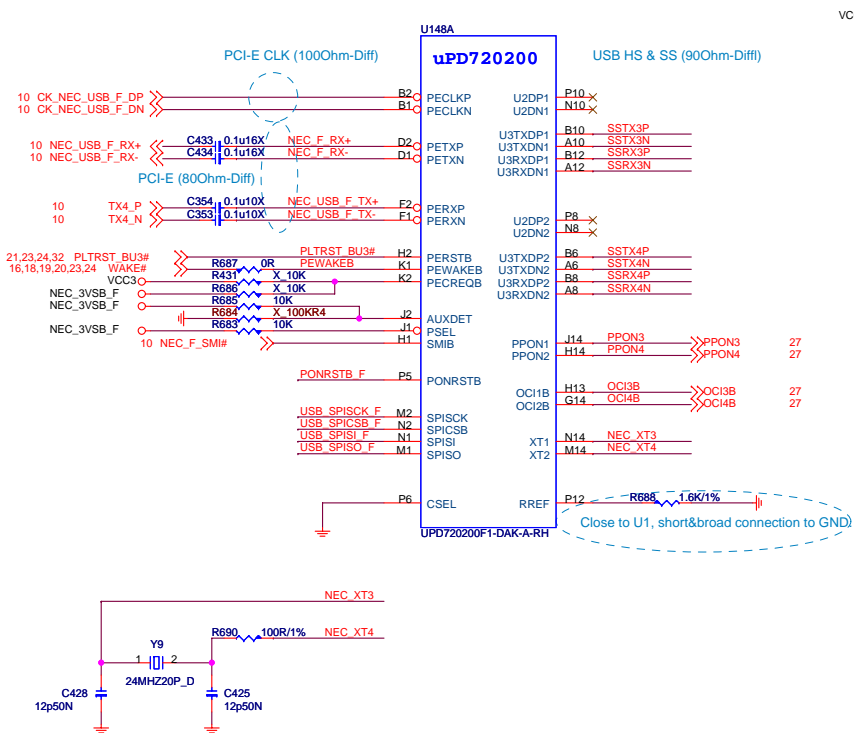
All power sources of uPD720200 are supplied, PPN0x is enable.
 PPN0x is low when OC0x going to low.

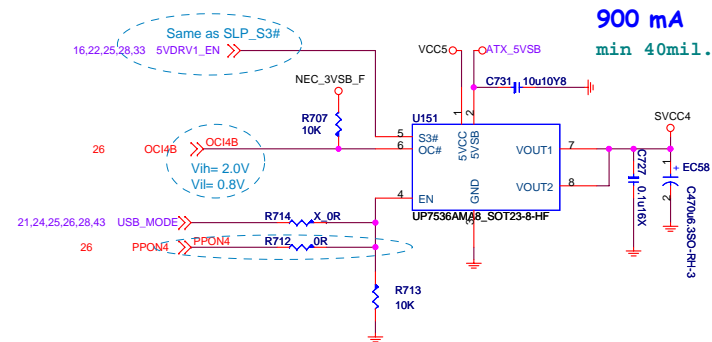
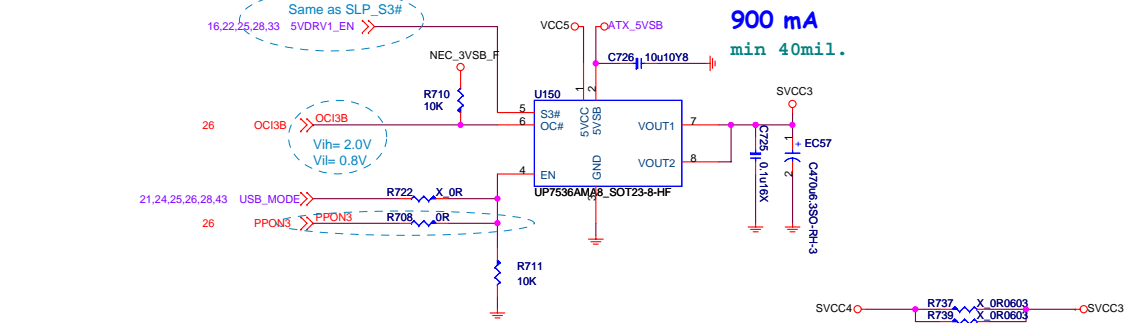
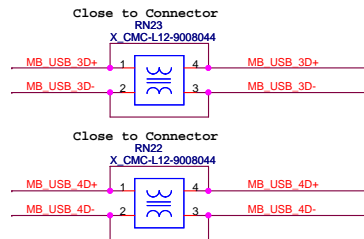
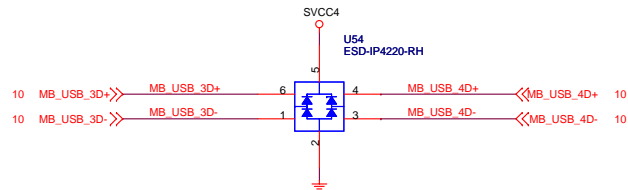
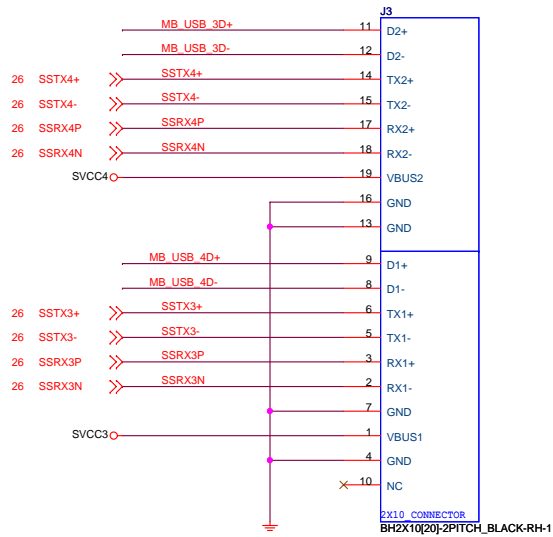


MICRO-STAR INT'L CO.,LTD

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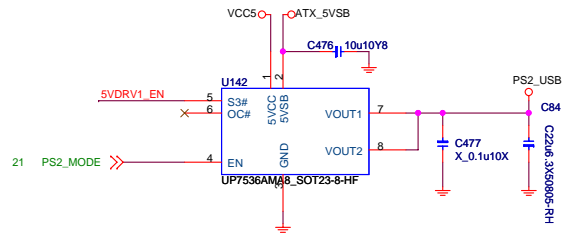
Size	Document Description	Rev
Custom	USB 3.0 Power & Connector	0A
Date: Sunday, August 22, 2010	Sheet 25 of 48	





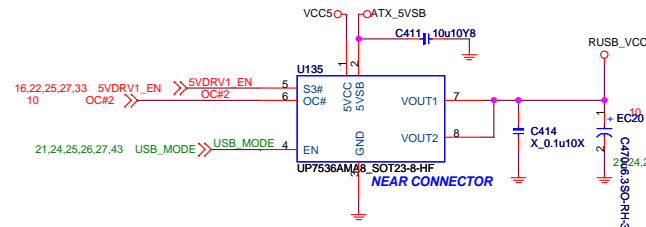
Front USB Connector

USB POWER FOR PORT 11,12

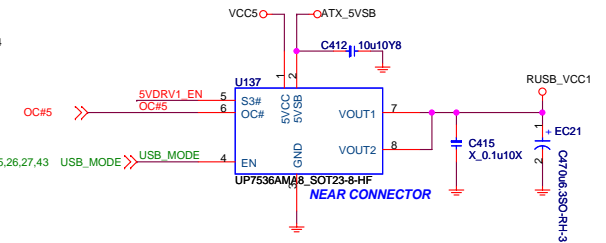


Rear USB Connector

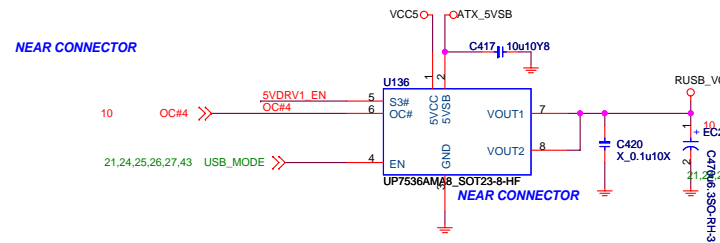
USB POWER FOR PORT 4,5



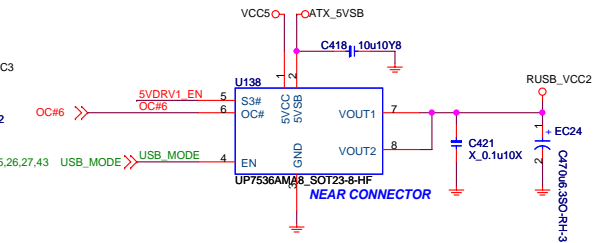
USB POWER FOR PORT 6,7



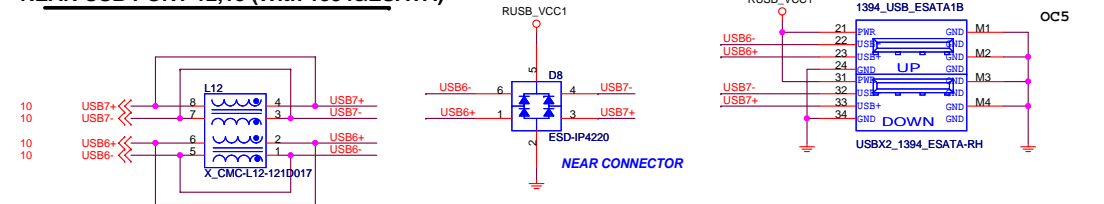
USB POWER FOR PORT 11,12



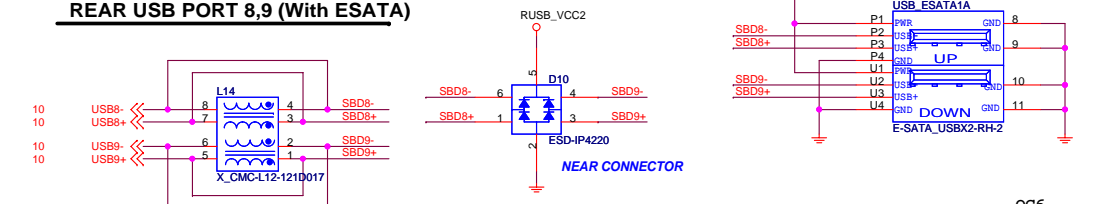
USB POWER FOR PORT 8,9



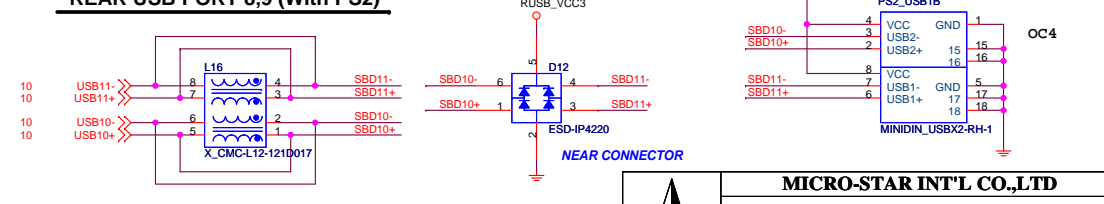
REAR USB PORT 12,13 (With 1394&ESATA)



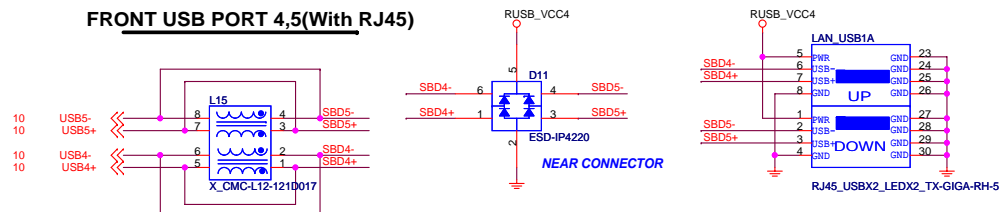
REAR USB PORT 8,9 (With ESATA)



REAR USB PORT 8,9 (With PS2)



FRONT USB PORT 4,5(With RJ45)



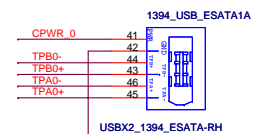
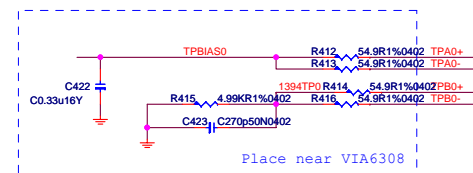
VT6308P - 1394 Controller

Trace Width/Spceing: 4/10/4

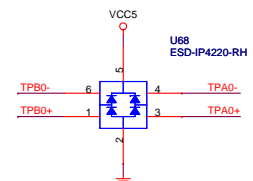
Impedance: 110 Ω / ± 6

Trace Length: < 6"

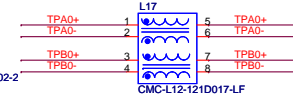
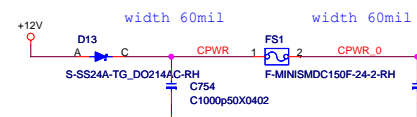
Rear 1394 port



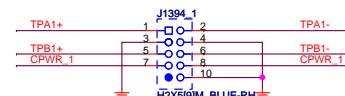
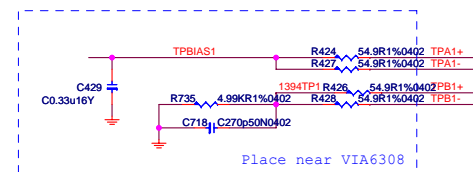
USBX2_1394_ESATA-RH



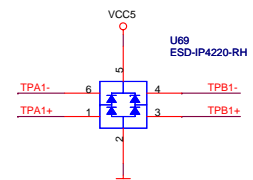
Close to Connector



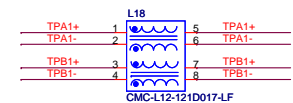
Front 1394 pin header



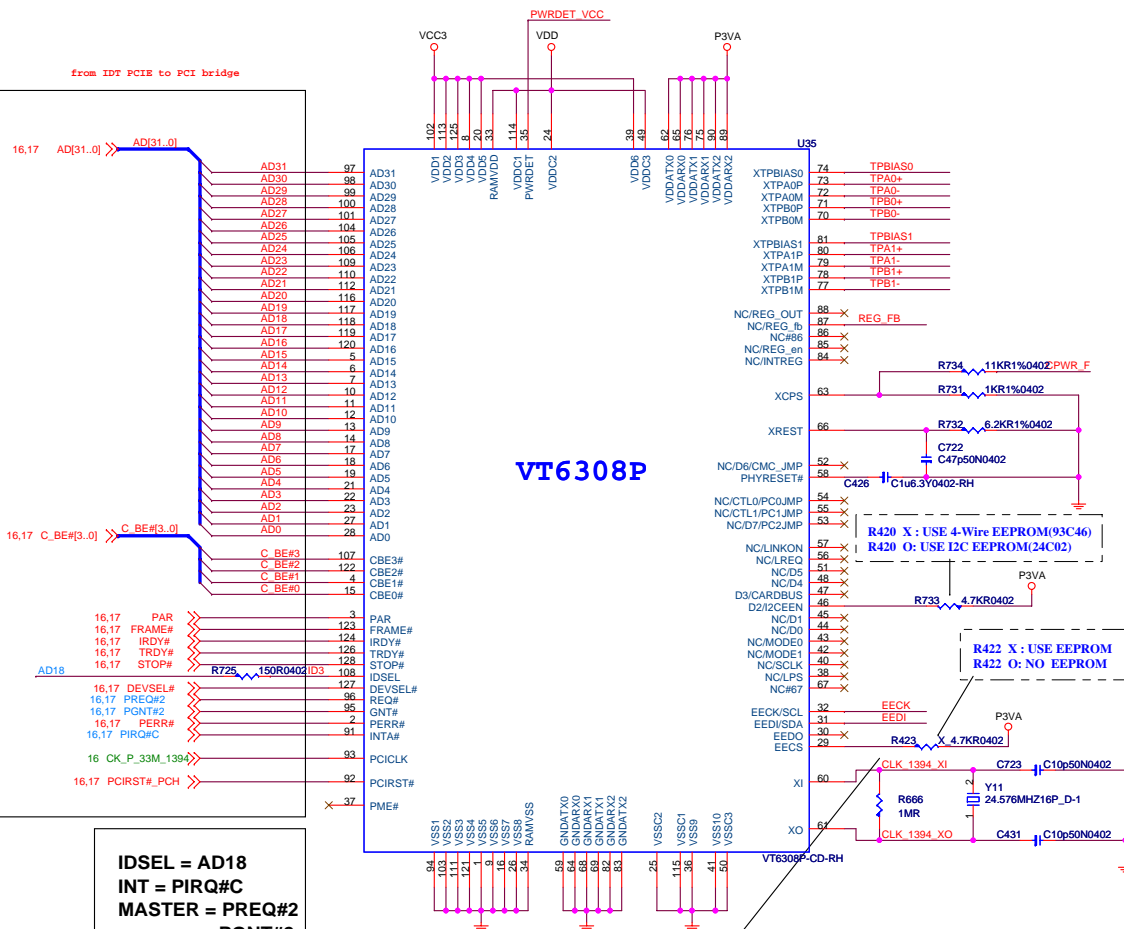
For Intel 1394 pinheader



Close to Connector



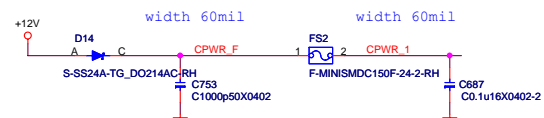
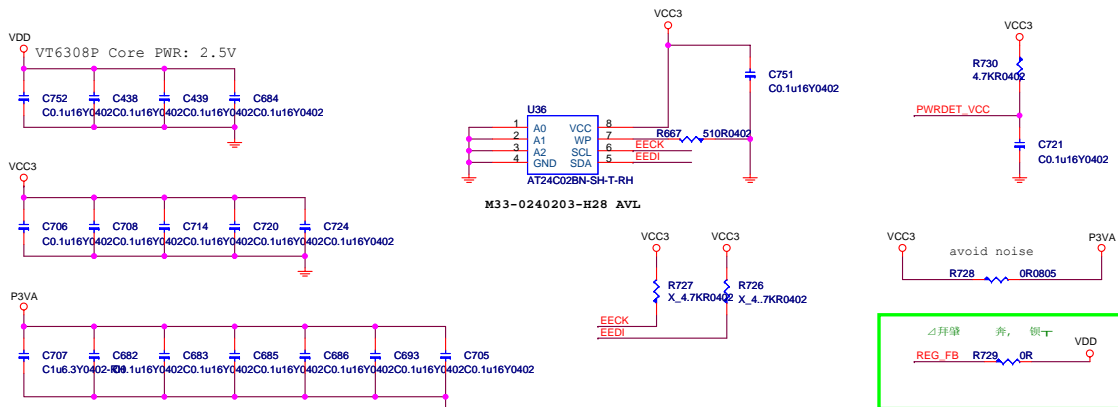
CMC-L12-121D017-LF



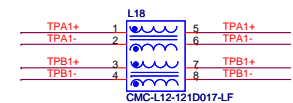
```

IDSEL = AD18
INT = PIRQ#C
MASTER = PREQ#2
PGNT#2

```



Close to Connector



CMC-L12-121D017-LF



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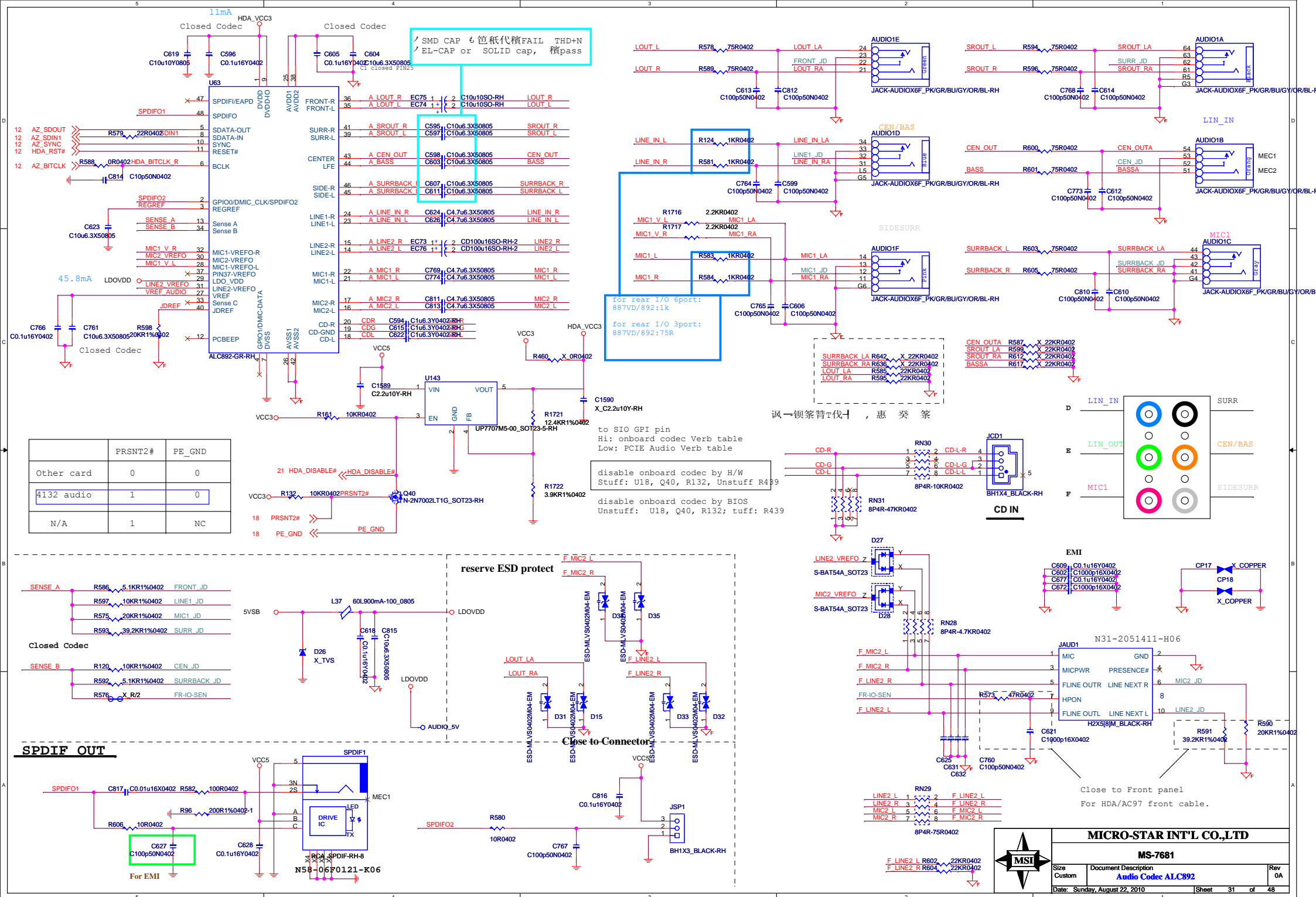
MS-7681

Size Custom	Document Description VT6308P-1394
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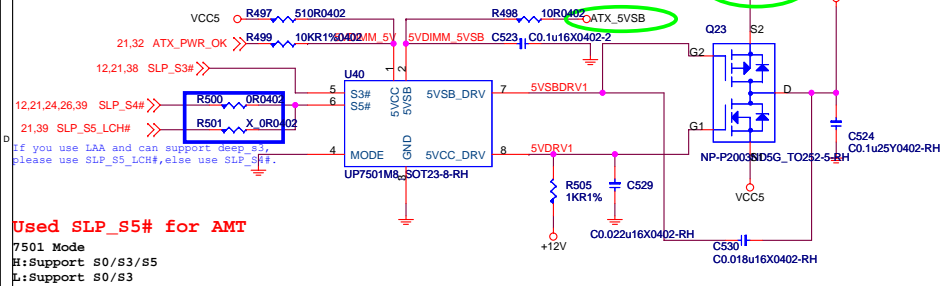
Rev	0A
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Date: Sunday, August 22, 2010

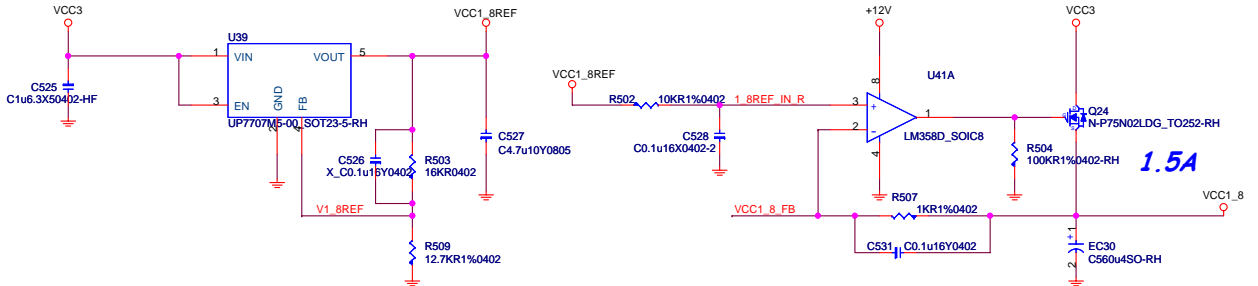
Sheet 29 of 48



5VDIMM FOR DDR



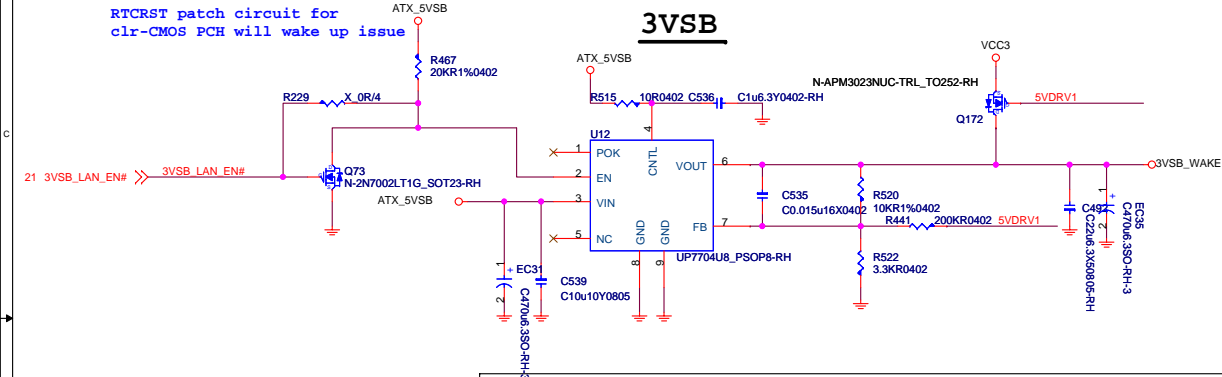
VCC1_8REF



3VSB_WAKE

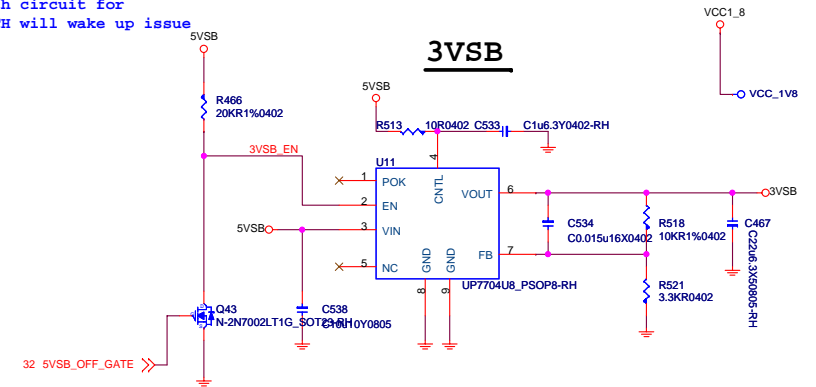
RTCST patch circuit for
clr-CMOS PCH will wake up issue

3VSB

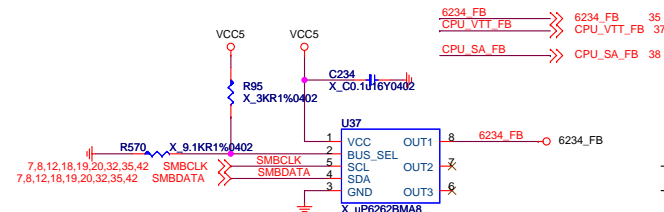
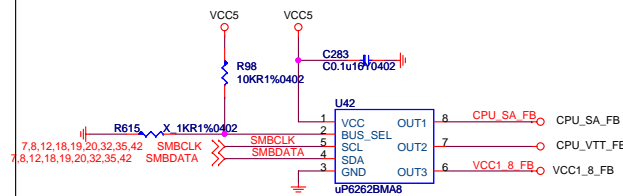
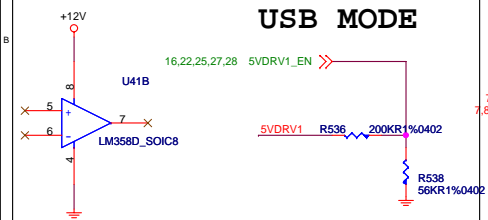


RTCST patch circuit for
clr-CMOS PCH will wake up issue

3VSB



USB MODE

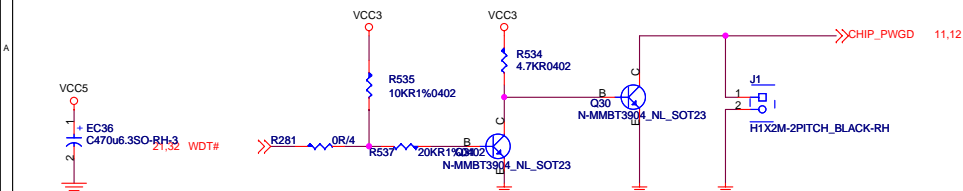


UPI VOLTAGE CONSOLE

0x20: RH=10K, RL=OPEN

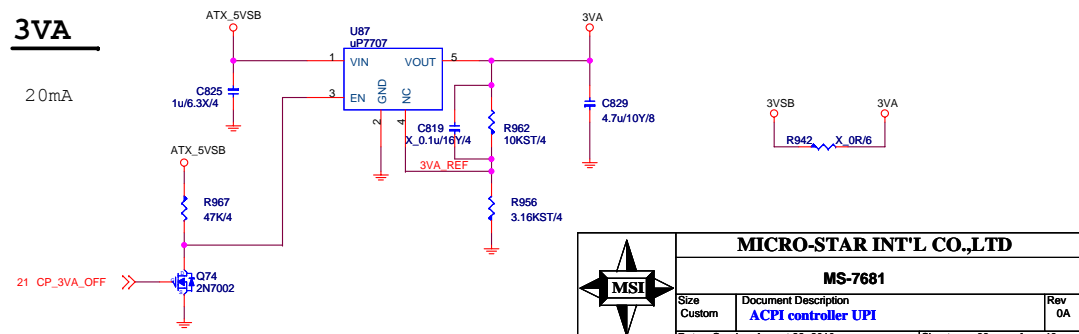
ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%

WATCH DOG

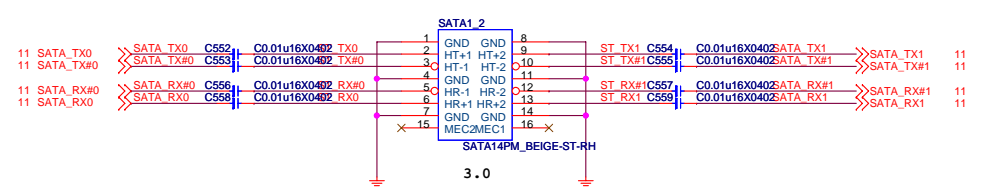
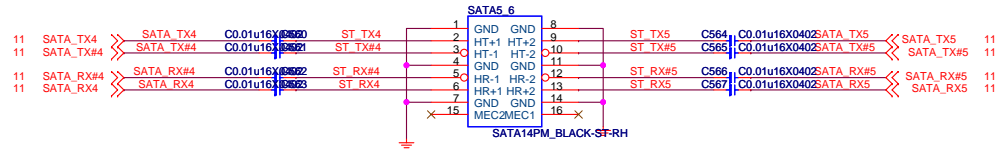
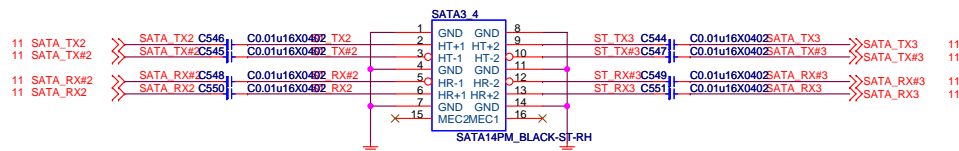
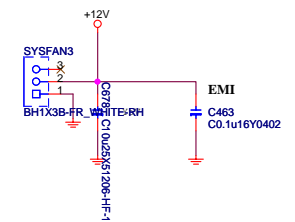
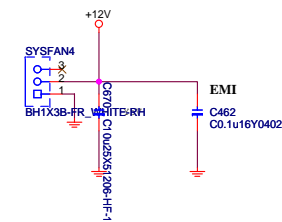
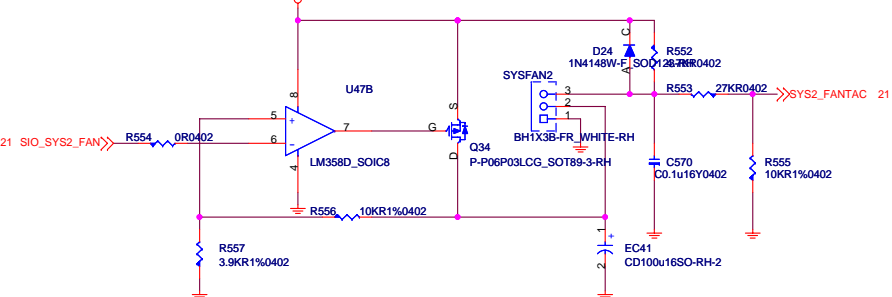
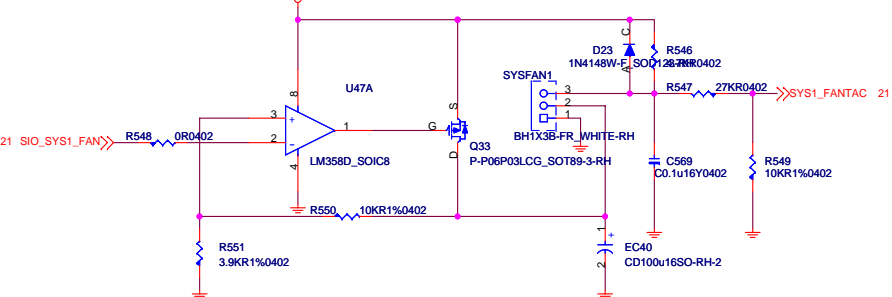


3VA

20mA

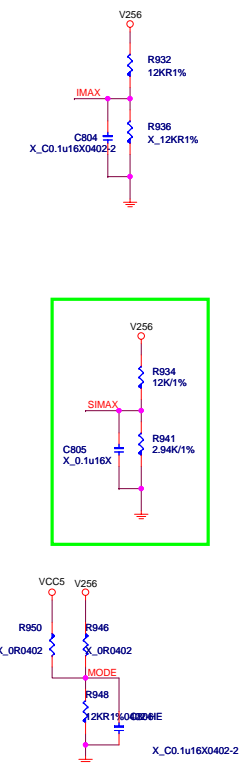
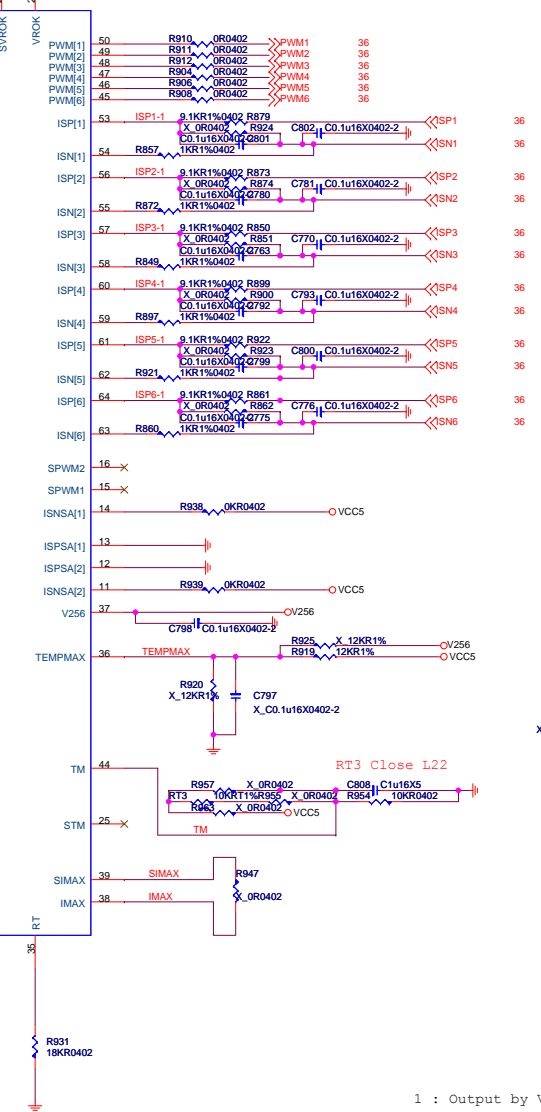
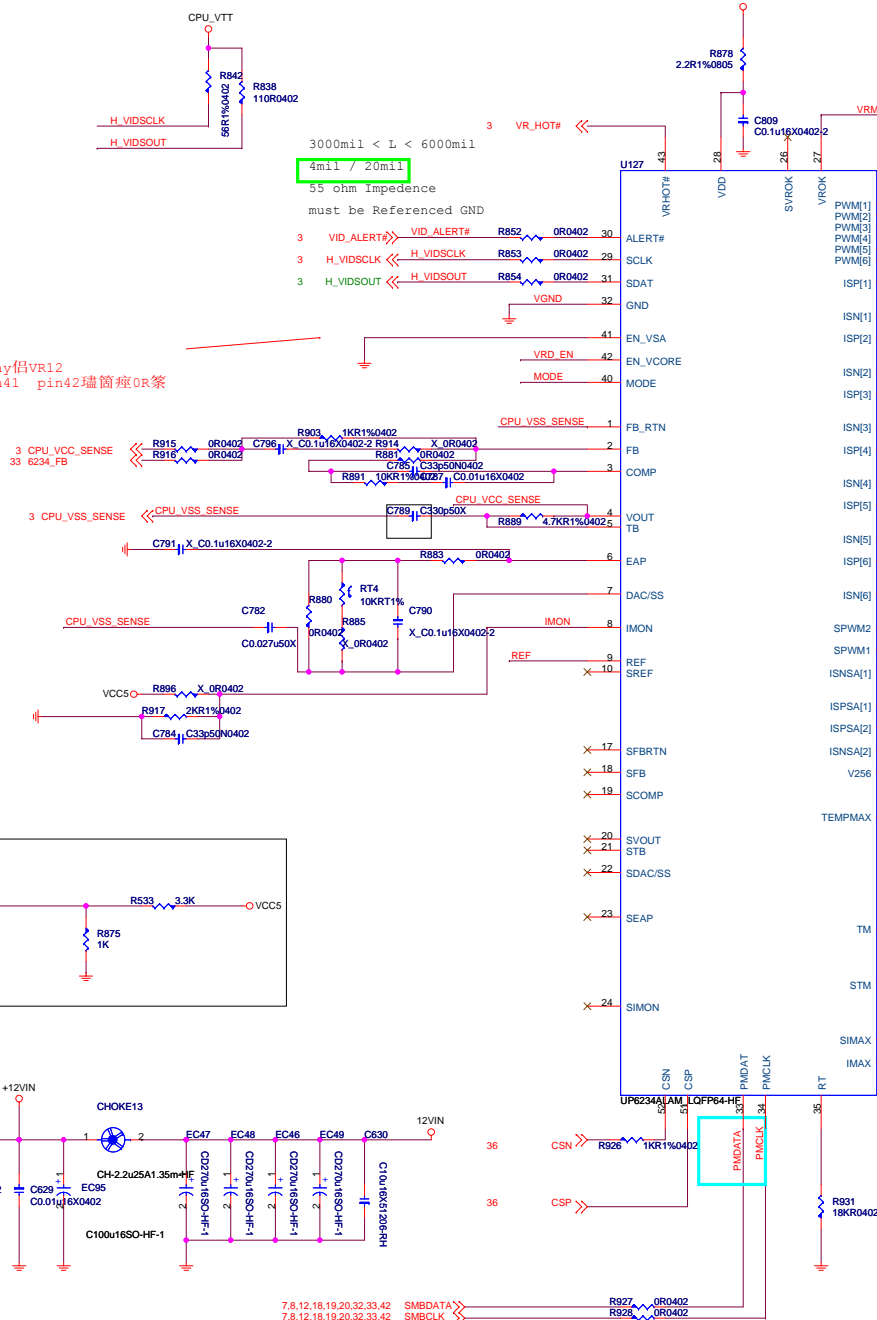
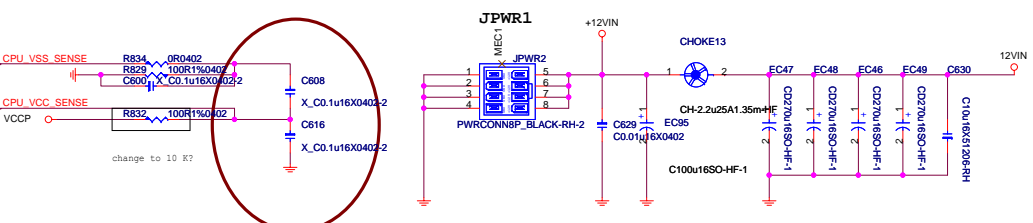
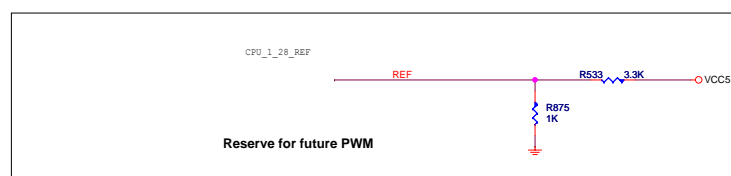
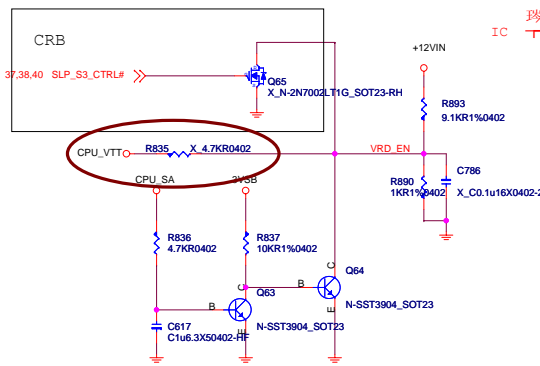


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Size	Document Description	Rev
Custom	ACPI controller UPI	0A
Date:	Sunday, August 22, 2010	Sheet 33 of 48

[illegible]

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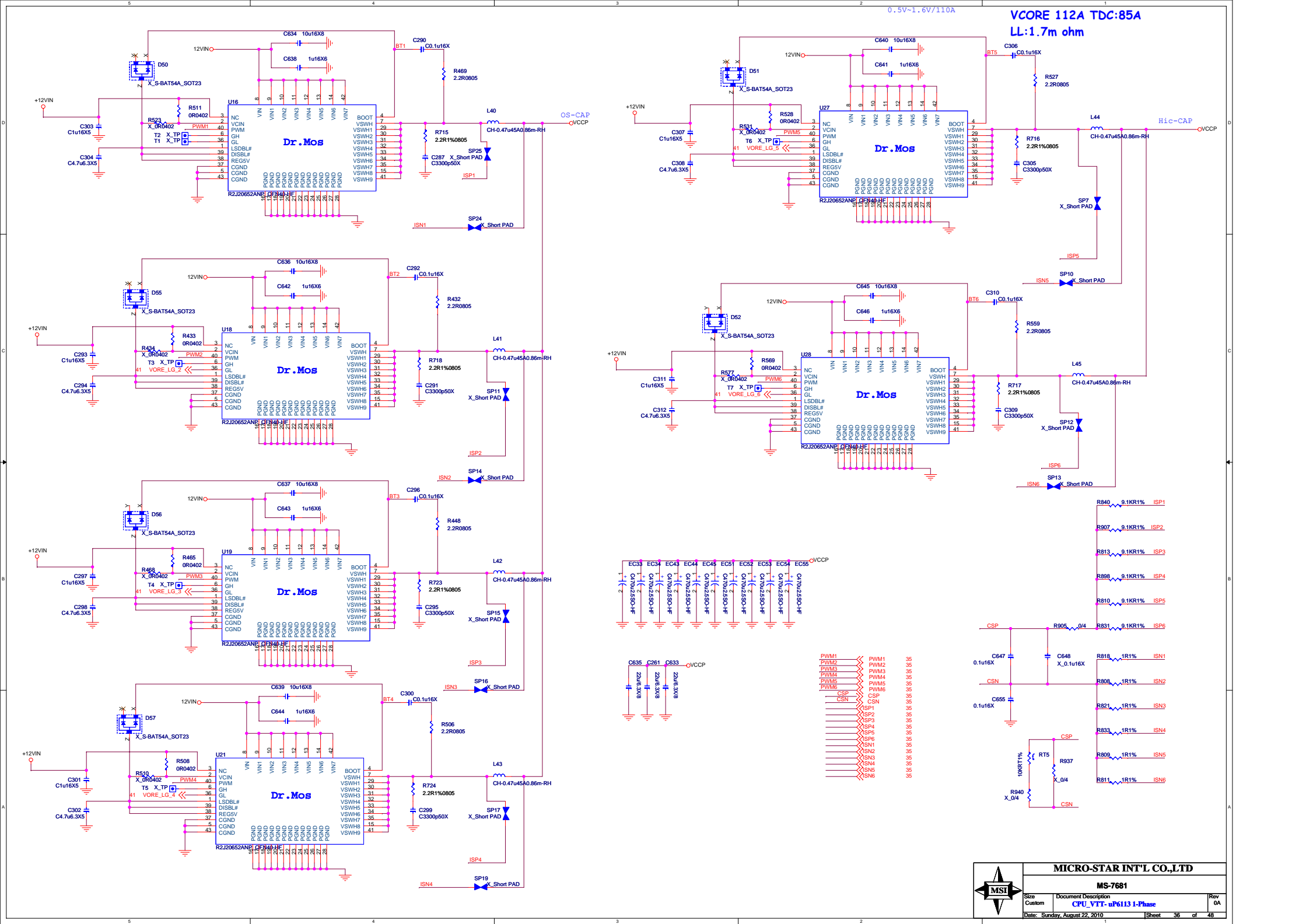
Size Custom	Document Description SATA & e-SATA Ports and Fan Control	Rev 0A
Date: Sunday, August 22, 2010		Sheet 34 of 48



1 : Output by Vref input



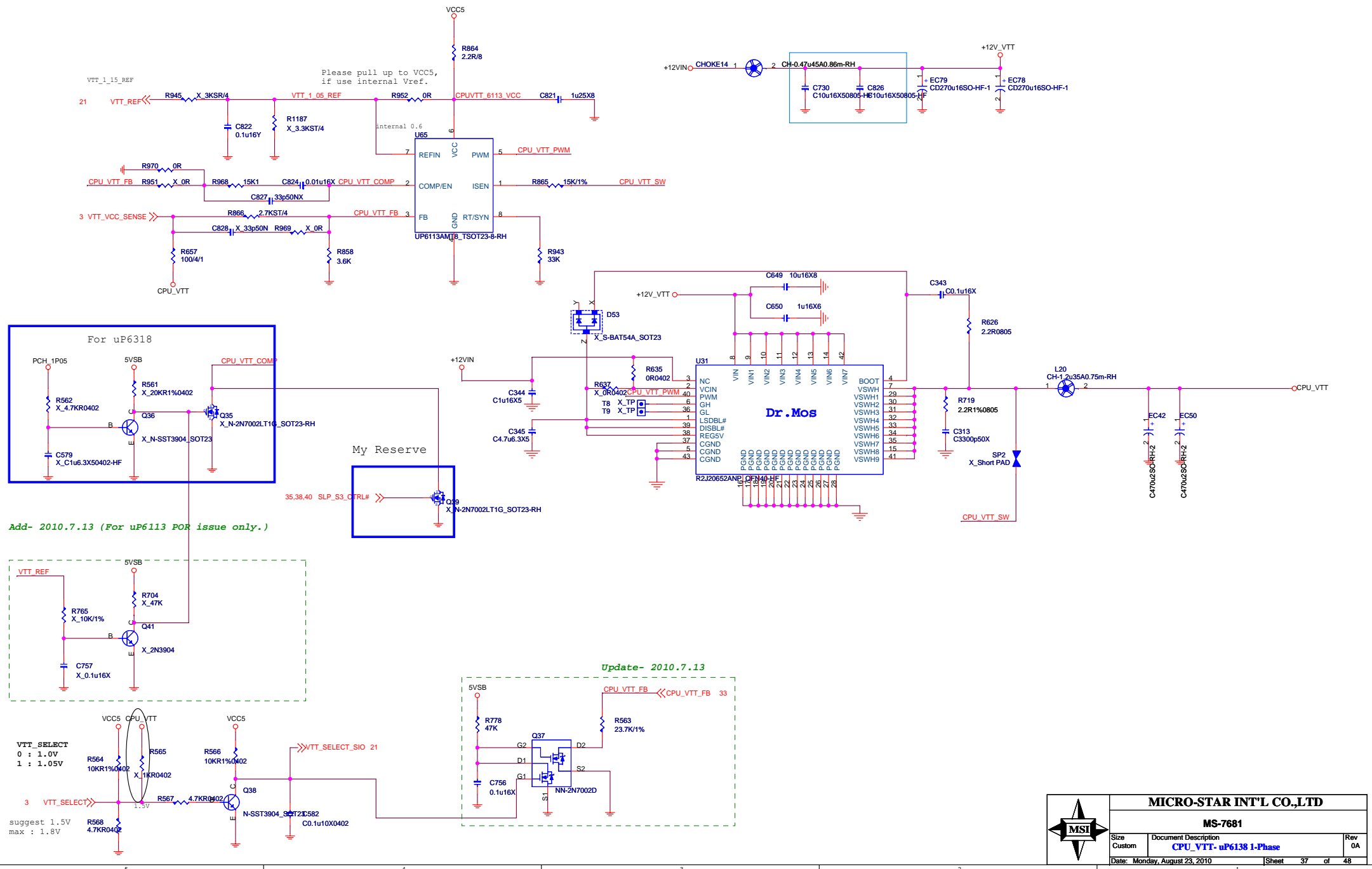
MICRO-STAR INT'L CO.,LTD			
MS-7681			
Customer	Document Description VRD12 - ISL6234 6+2Phase	Revision 0.	
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CPU_VTT:1.05/1.00

CPU VTT 8.2A

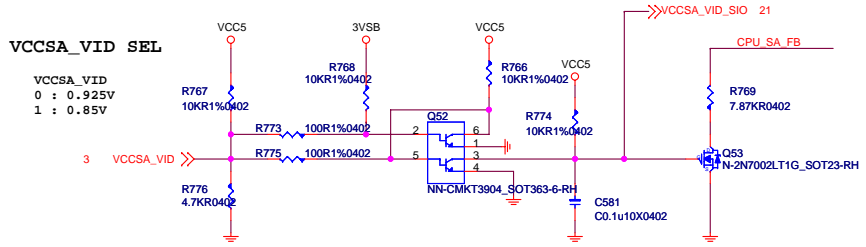
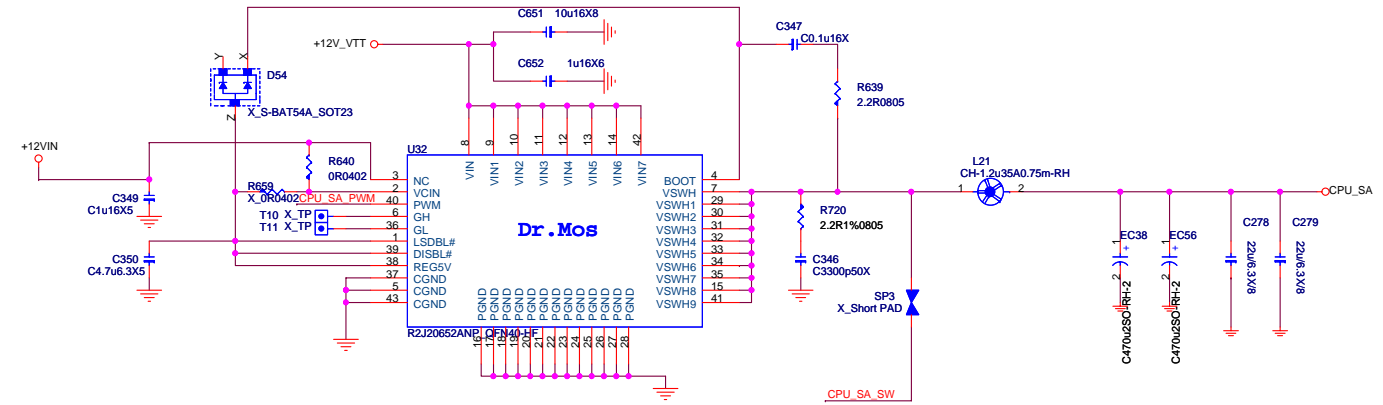
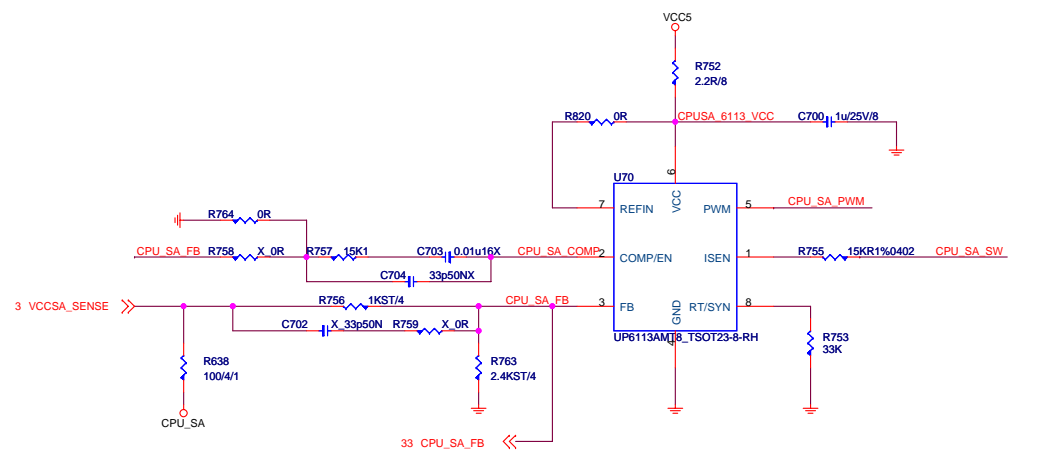
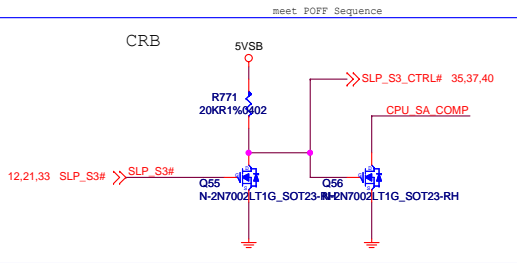
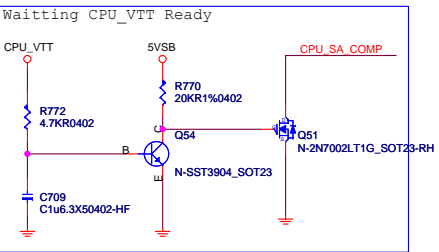
$$\begin{aligned} \text{Tripple} &= 1.9(\text{vtt}) + 1.8(\text{sa}) \\ 5 \times 2 &= 10\text{A} > 3.8\text{A} \end{aligned}$$



MICRO-STAR INT'L CO.,LTD		
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Custom	CPU_VTT- uP6138 1-Phase	0A
Date: Monday, August 23, 2010	Sheet 37 of 48	

CPU_SA:0.925/0.85

SA Core =8.8A



VCCSA_VID	
Low	0.925V
High	0.85V

VCCSA_VID_SIO Table	
Low	0.85V
High	0.925V

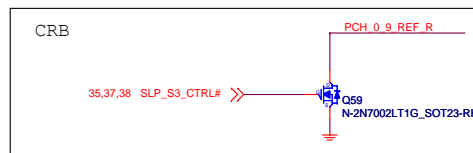
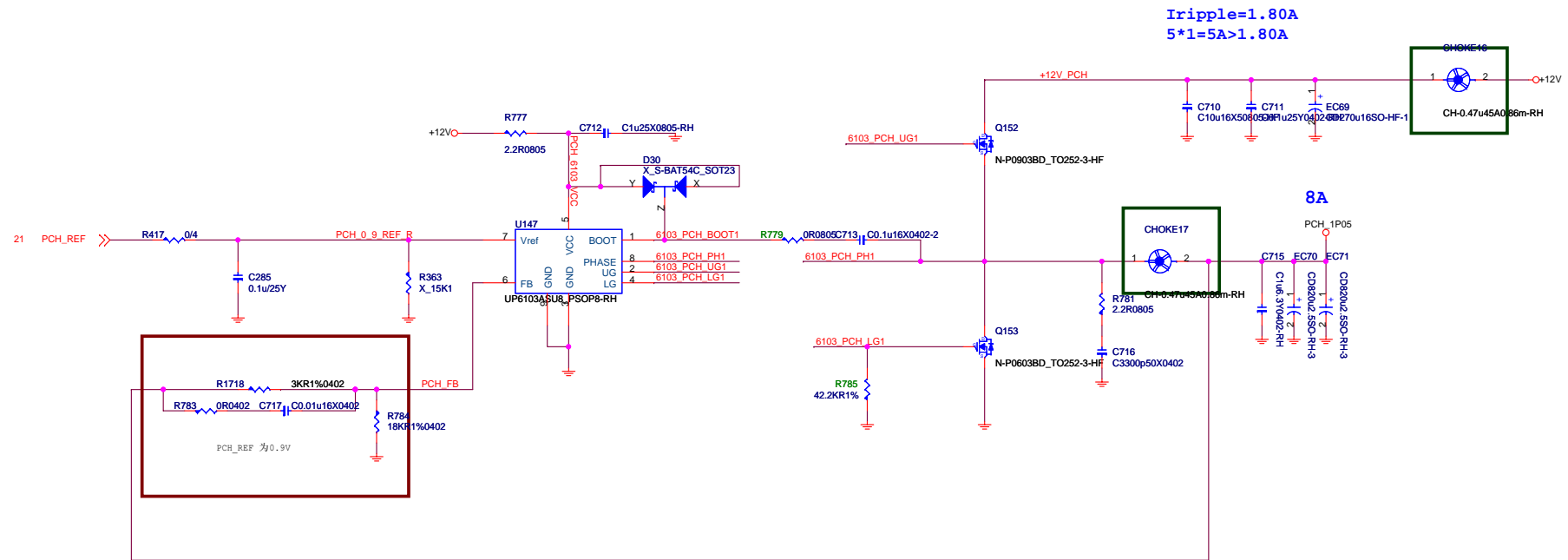
MICRO-STAR INT'L CO.,LTD		
MS-7681		
Size Custom	Document Description CPU_SA-uP6113-1Dr.MOS	Rev 0A
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4.5A FOR CPU
15A FOR 4DIMM
1A FOR DDR VTT



MICRO-STAR INT'L CO.,LTD			
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PCH Core $6.2A + 1.8A = 8A$



	uP6103A	uP6138
PIN1	BOOT	BOOT
PIN2	UG	UG
PIN3	GND	VREFIN
PIN4	LG	LG
PIN5	VCC	VCC
PIN6	FB	FB
PIN7	Vref	OCF/EN
PIN8	PHASE	PHASE
PIN9	GND	GND

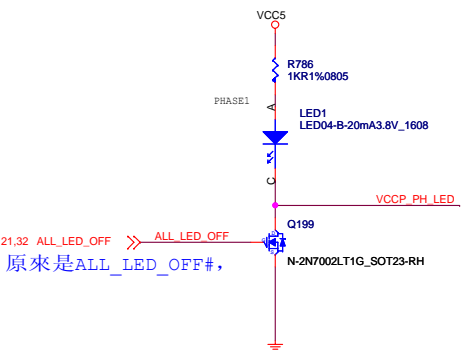


MICRO-STAR INT'L CO.,LTD

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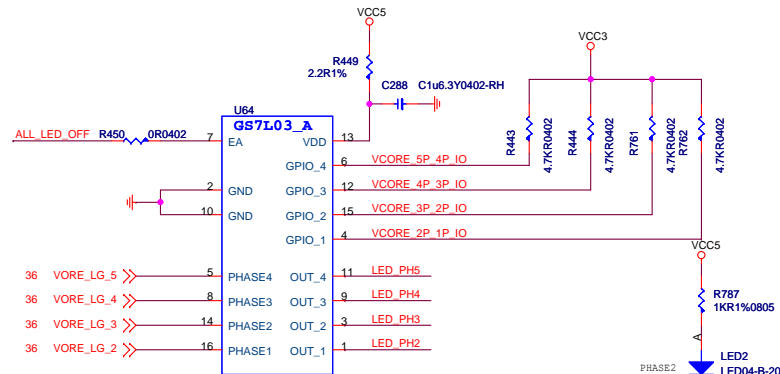
Size Custom	Document Description PCH Power - uP6103 1-Phase	Rev 0A
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all on board LED switch

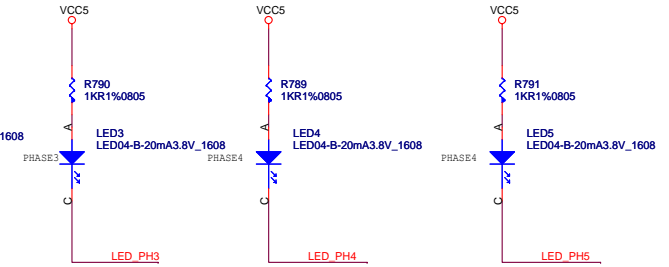
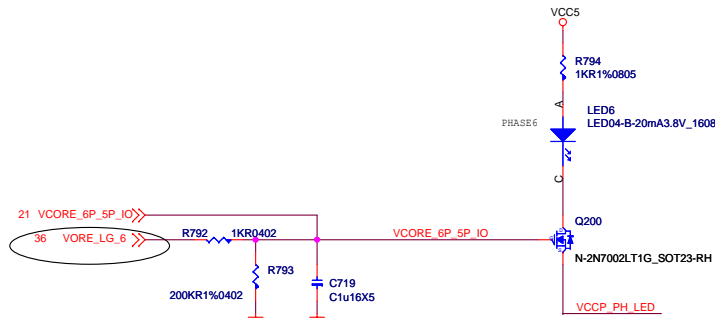


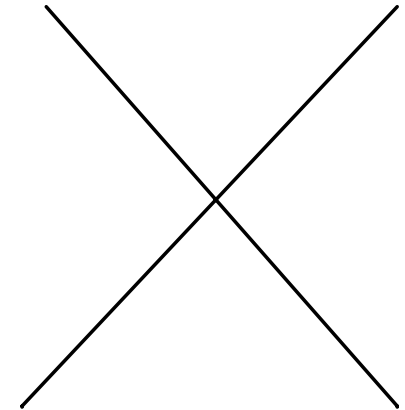
21,32 ALL_LED_OFF >> ALL_LED_OFF
原來是ALL_LED_OFF#.

21 VCORE_5P_4P_IO >> VCORE_5P_4P_IO
21 VCORE_4P_3P_IO >> VCORE_4P_3P_IO
21 VCORE_3P_2P_IO >> VCORE_3P_2P_IO
21 VCORE_2P_1P_IO >> VCORE_2P_1P_IO



36 VORE_LG_5 >> PHASE4 OUT_4 11 LED PH5
36 VORE_LG_4 >> PHASE3 OUT_3 9 LED PH4
36 VORE_LG_3 >> PHASE2 OUT_2 3 LED PH3
36 VORE_LG_2 >> PHASE1 OUT_1 1 LED PH2





Mounting Holes

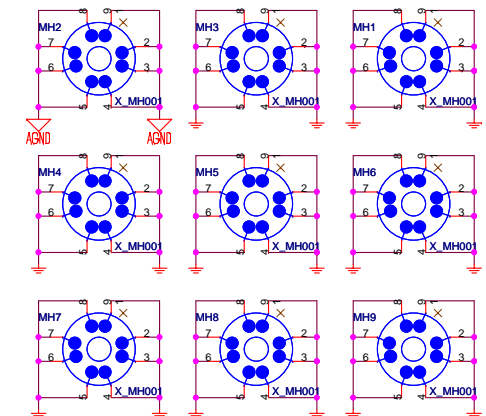
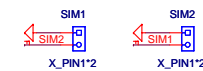


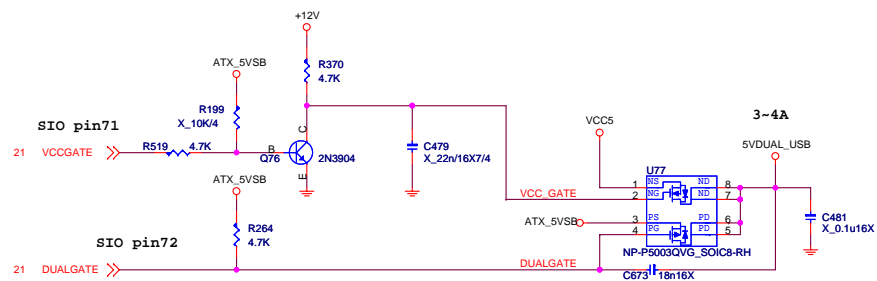
Diagram showing eight FM (Frequency Modulation) signals, labeled FM1 through FM8, each with a corresponding X_FM label below it.

Diagram illustrating the HS-0404592-RH component assembly. The assembly consists of a main component (HS-0404592-RH) connected to a power source (U4_X1) and a load (U4_X2).

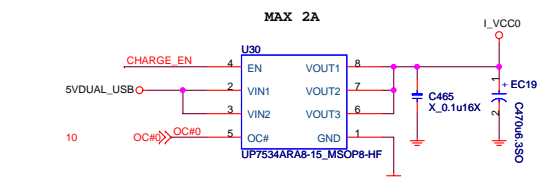


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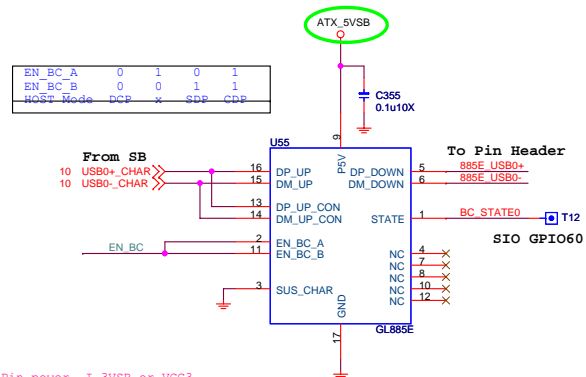
5VDUAL_USB



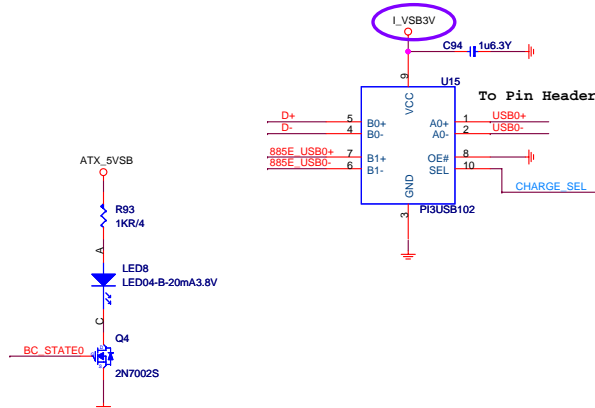
USB POWER FOR PORT 0 for Battery Charging



2010.06.08



Pin power I_3VSB or VCC3
Register power I_3VSB or VCC3
Register reset I_3VSB or LRESET#



SIO GPIO40 Pin7 (VBAT for New F71889AD)

USB_CHARGE:

0: Don't support USB charge and resume.
1: Support USB charge and resume.

1st boot , H/W default support USB charge.

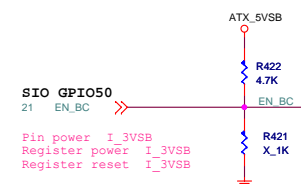
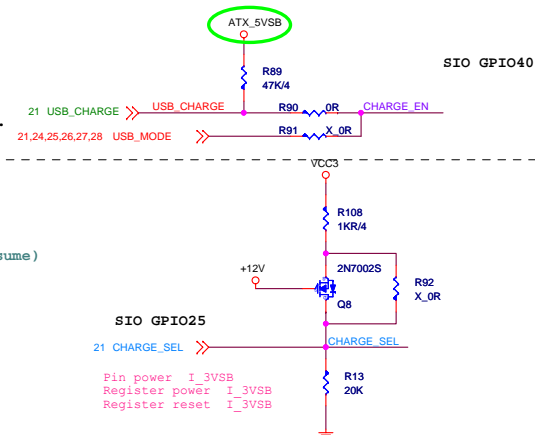
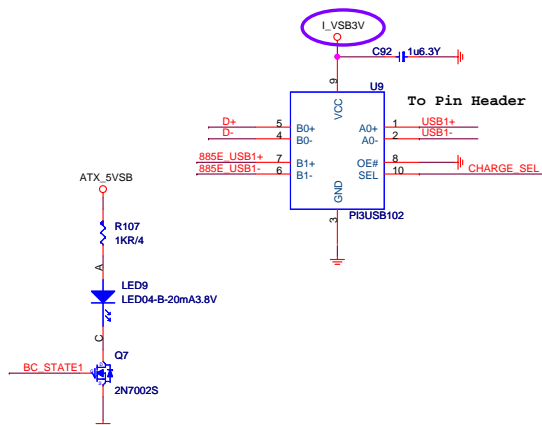
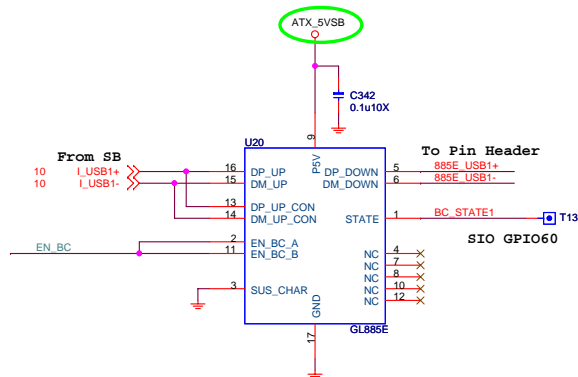
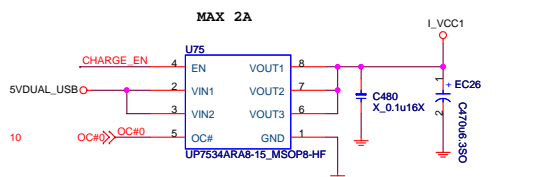
SIO GPIO50 (I_VSB3V)

BC_SEL: (PUSH PULL)

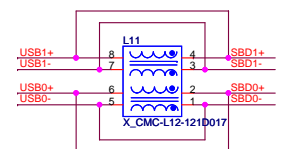
```
0: Support DCP device(don't support usb link and resume)
1: Support CDP (Support usb link and resume)
```

1st boot , H/W default support DCP.

USB POWER FOR PORT 1 for I charge



FRONT USB PORT 0,1

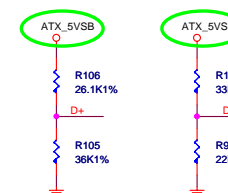
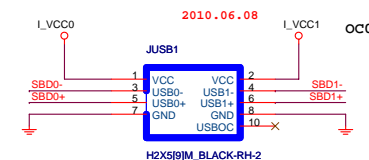


SIO GPIO pin 15

Default low

LOW= support I charge

1st boot H/W default support i charge



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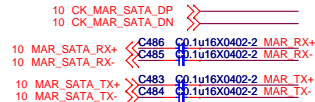
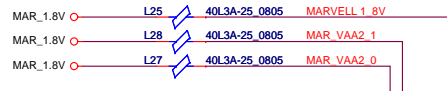
Size
Custom

Document Description
USB CHARGER

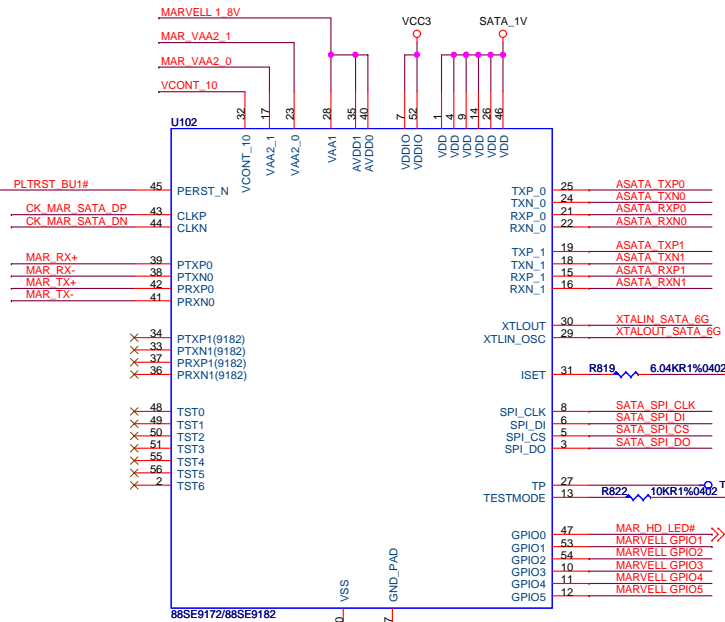
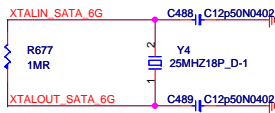
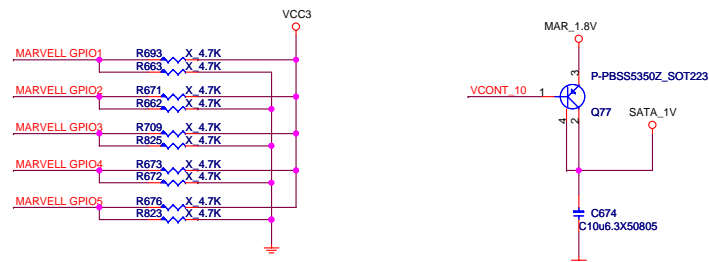
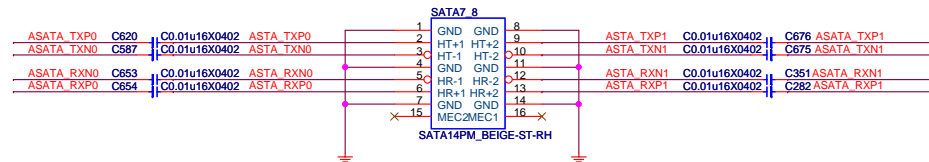
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Date: Sunday, August 22, 2010

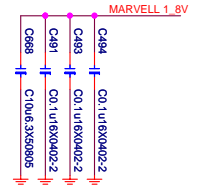
Sheet 43 of 48



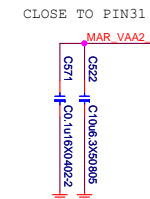
SATA 6G PORT 7,8



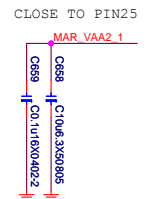
SATA_1.8V 100 mA



SATA_VAA2_0 70mA

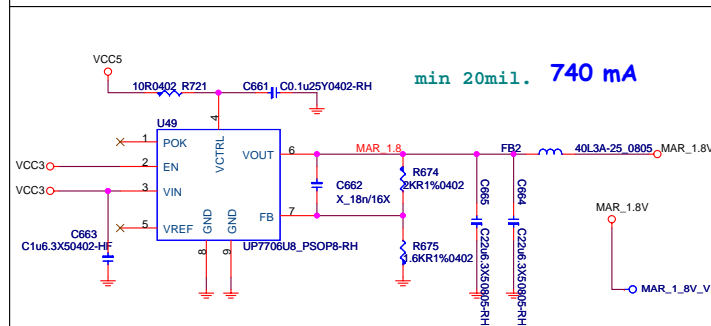
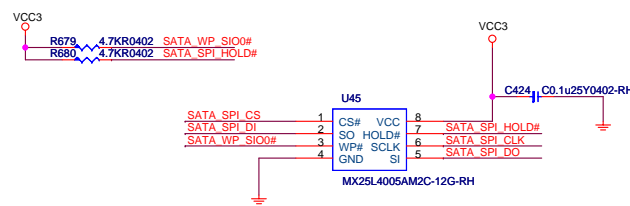
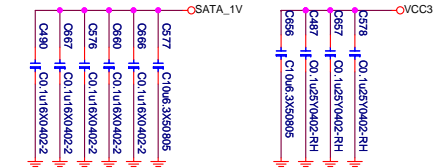


SATA_VAA2_1 70mA



SATA_1V 500 mA

CLOSE TO PIN5, 13, 21, 51, 64, 71



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Custom	MARVELL SATA 6G	0A
Date: Sunday, August 22, 2010	Sheet 44 of 48	